Low-power Bluetooth Microcontroller Design Using Clock Gating and Gray Code State Encoding

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Abstract. The number of applications for wireless Bluetooth devices is on the rise this decade. However, power consumption has become a major concern as the demand for more functionality on a single chip increases. Furthermore, since the device has a limited battery capacity, high power consumption limits the chip's long-term operation. Therefore, low-power architecture becomes crucial in these devices. To minimize the power consumption, this work implements a clock gating and a Gray code state encoding in a Bluetooth microcontroller system-on-chip (SoC). Four operation state is being tested to measure switching activity: Bluetooth transmission test, sleep test, timer test, and UART test. This design targets 180 nm Silterra CMOS technology with the system working at 16 MHz. Synopsys System on Chip EDA tools is used to perform the gate-level simulation and power analysis. The experimental result showed that the system's power consumption decreased by 84% when applying clock gating. Implementing a Gray code state encoding on the bridge reduces the power consumption further by up to 42 µW.

INTRODUCTION

Nowadays, many smart appliances are controlled via a Bluetooth microcontroller. According to [1], there were around 4 billion devices powered by Bluetooth in 2018. Its low-power consumption makes it popular for transferring small data [2]. However, wireless devices are typically designed to be portable and have a limited battery capacity. Furthermore, high power consumption can lead to a rise in device operating temperature. This can reduce the reliability of the device. Hence, it is essential to design a device that uses as little power consumption as possible [3].

To reduce the power consumption of these devices, this work implement clock gating and gray code state encoding into a wireless system-on-chip (SoC) Bluetooth microcontroller. The system is targeted for SilTerra 180nm CMOS technology and is validated using a hardware-software co-verification approach. Different components or IP blocks are integrated into the system architecture. The power analysis is estimated based on the system's switching activity using Synopsys System-on-Chip EDA tools.

This paper is arranged as follows. The introduction of the Bluetooth System-on-Chip (SoC) microcontroller is discussed in the Literature Review section. The low power methodology implemented in this paper is presented in the Methodology section. The results are presented in the Result and Discussion section. Finally, the Conclusion section summarizes the finding of this paper.

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LITERATURE REVIEW

The advancement of wireless microcontroller technology has encouraged the spread of the Internet of Things (IoT), which connects various devices to the internet. Reliability, low power consumption, and high transmission rates are among the deciding factors in network choice [6]. One wireless technology is ZigBee, based on IEEE 802.15.4 standard. It can be found in many applications, such as smart homes, agriculture, and medical. A CC2430 ZigBee SoC from Texas Instrument (TI) is used as an indoor home security system in [7], where various sensors are employed to monitor the home ambient in a real-time monitoring system.

In [8], Bluetooth Low Energy (BLE) achieved the lowest power consumption in the comparison between ZigBee and ANT in a cyclic sleep event. However, the power consumption for ZigBee is higher compared to Bluetooth wireless technology. The comparison is made by sending the same packet size data and transmission distance using CC2540 from TI and XBee S2 from Digi International.

Three different wireless sensor network using BLE and Wi-Fi for noise monitoring is developed in [9]. The prototype uses RFD 22301, BMD-200 BLE SoC, and Wi-Fi Spark Core embedded board as the sensor network connects to a Raspberry Pi gateway. Based on the paper, the BMD-200 node has achieved the lowest power consumption and almost half of the Wi-Fi transmission range. Its ease of connectivity and the high sampling rate has made BLE the preferred choice to be deployed in IoT application.

Wireless sensor communication using a Wi-Fi-based sensor network is implemented in IoT by [10]. The design used CC3220SF as a transaction verifier for a blockchain-based payment in IoT. Research in [11] for senior citizen's home surveillance also uses the same Wi-Fi SoC devices as the sensor node. The collected data are sent to regional health professionals without a dedicated internet hub. However, this method that uses Wi-Fi as a sensor node can cost a lot of power consumption. Analysis by [12] shows that the power consumption using RN-131C/G (Wi-Fi) is higher than CYBLE-022001-00 (BLE).

TABLE 1. Comparison Wireless Microcontroller SoC.

References	**[7]**	**[8]**	**[10]**	**[9]**	**[12]**
SoC Brand	CC2430 TI	CC2540 TI	CC3220 TI	BMD-200 Rigado	CYBLE-022001-00 Cypress
Processor	8051	8051	Cortex-M4	Cortex-M0	Cortex-M0
RF Technology	ZigBee	BLE 4.2	Wi-Fi	BLE 4.2	BLE 4.2
Peripherals	USART, Timer, Watchdog, AES	USART, Timer, Watchdog, AES, GPIO	UART, SPI, I^2C, Timer, Watchdog, GPIO, HTTP	UART, SPI, Watchdog, AES-128, TDSP, GPIO	UART, SPI, Watchdog, AES-128, TDSP, GPIO
Frequency	32 MHz	32 MHz	40 MHz	16 MHz	48 MHz
Rx	27 mA	15.8 mA	59 mA	9.7 mA,	18.7 mA
Tx	27 mA	18.6 mA	272 mA	11.8 mA,	15.6 mA
Data Rate	250 kbps	1 Mbps	16 Mbps	1 Mbps	1 Mbps
Range	0 dBm	+4 dBm	+18 dBm	+4 dBm	+3 dBm
Application	Home Security	(Analysis)	IoT Blockchain Payment	Noise Monitoring	Environmental Monitoring

According to [16], one of the best ways to reduce power consumption in an integrated circuit is to turn off the part that is not in use. The VLSI circuit's power consumption consists of static and dynamic power since the logic gates do not typically switch every clock cycle. Switching activity and clock frequency heavily affect the average power consumption. However, the challenge is to reduce the number of switching transistors without affecting the system functionality [17]. For this purpose, clock gating effectively reduces unwanted energy wastage at the clock network. Research in [18] reduced the dynamic power consumption in the OpenRisc on-chip system by using clock gating. The author claimed that a reduction of about 50% to 80% of power consumption is achieved for different components after implementing the clock gating.

The other method that can reduce the switching activity is by using Gray coding. Research by [19] utilizes the Gray code in Wireless Sensor Network (WSN) for low-power communication protocol. In [20], the authors proposed a steganography method using Gray code for the images. Research [21] uses Gray Code in Finite State Machine (FSM) in the IoT application. According to [22], FSM is one of the crucial parts of a sequential design. Research by [23] also claims that efficient FSM design techniques are important. Table 2 shows the comparison between Gray code and binary digits. The bit transition in binary digit occurs depending on the state, while for Gray code, only one-bit transition per state transition is allowed. In other words, the Hamming distance between adjacent Gray codes is always one [24]. The lower the number of bit transitions in FSM, the lower the dynamic power consumption [25] [26].

TABLE 2. Comparison of Binary and Gray Code Transformations.

State	Binary Code				Transition	Gray Code				Transition
	Q3	Q2	Q1	Q0		Q3	Q2	Q1	Q0	
0	0	0	0	0		0	0	0	0	
1	0	0	0	1	1	0	0	0	1	1
2	0	0	1	0	2	0	0	1	1	1
3	0	0	1	1	1	0	0	1	0	1
4	0	1	0	0	3	0	1	1	0	1
5	0	1	0	1	1	0	1	1	1	1
6	0	1	1	0	2	0	1	0	1	1
7	0	1	1	1	1	0	1	0	0	1
8	1	0	0	0	4	1	1	0	0	1

METHODOLOGY

Figure 1 shows the overall block diagram for our wireless Bluetooth microcontroller design. The design consists of an ARM Cortex-M0 processor, a Bluetooth processing unit, and other peripherals such as a timer, watchdog, and RTC. In this work, the design is mapped to Silterra 180nm CMOS technology before it is simulated at gate-level simulation using Synopsys System-on-Chip EDA Tools.

Four tests are chosen to evaluate the power consumption of the system: the Bluetooth transmit test, the sleep test, the timer test, and the UART test. These tests are expected to have different switching power activities. A clock gating is implemented to the full chip on the clock network to reduce power consumption. The clock for the system will be disabled when it is not being used, such as when the system is in sleep mode or idle state. The clock gating uses a latch and an AND gate to control the clock. Fig. 2 shows the flow for analyzing power consumption using a Power Compiler from Synopsys.

In this design, APB Bridge is important to connect the peripherals and the processor since much data are transferred between these two modules. Hence, reducing switching activity on the bridge can reduce power consumption. As discussed in the previous section, Gray code is a coded binary representation that only allows one bit changed for consecutive digits to reduce the switching activity. In this work, a Gray code state encoding is implemented in the FSM of the system bus bridge, as shown in Fig. 3.

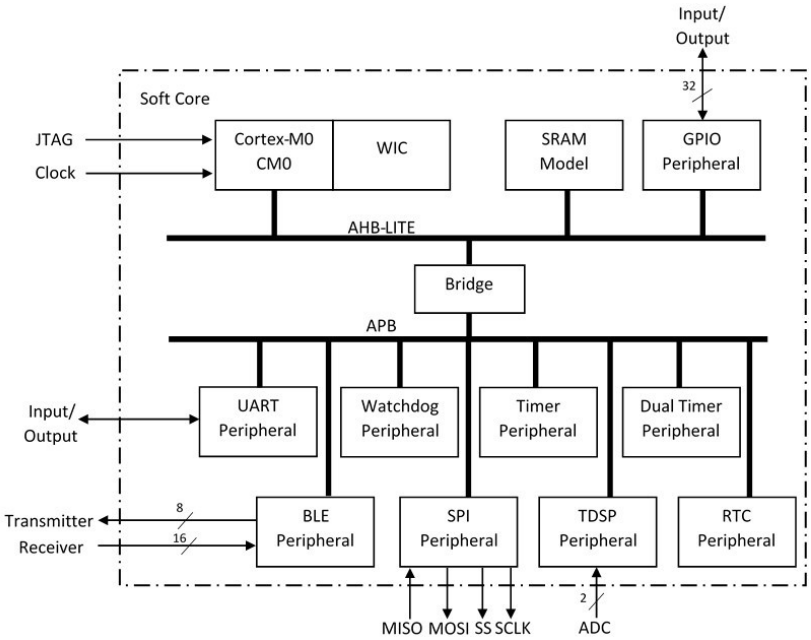

FIGURE 1. Block diagram for the Bluetooth microcontroller system.

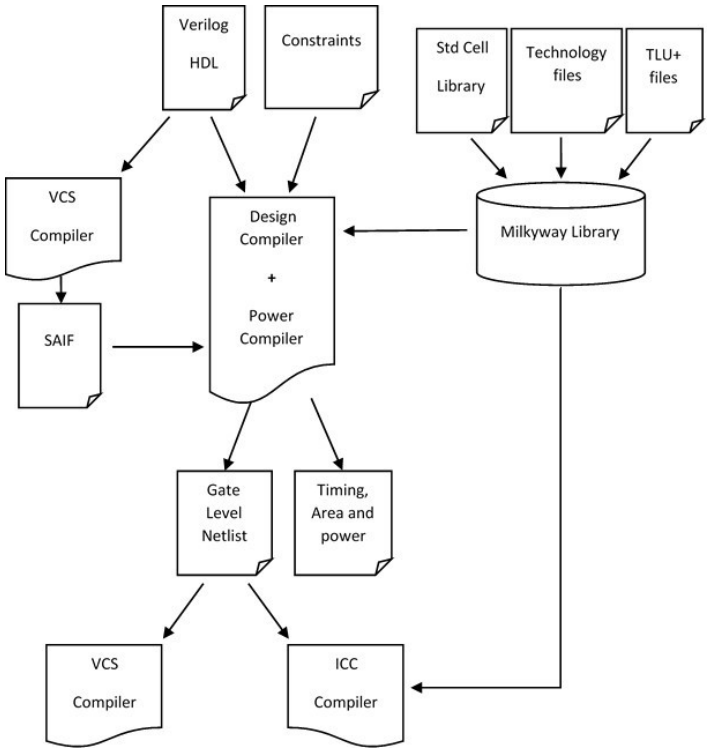

FIGURE 1. Power Analysis flow [27].

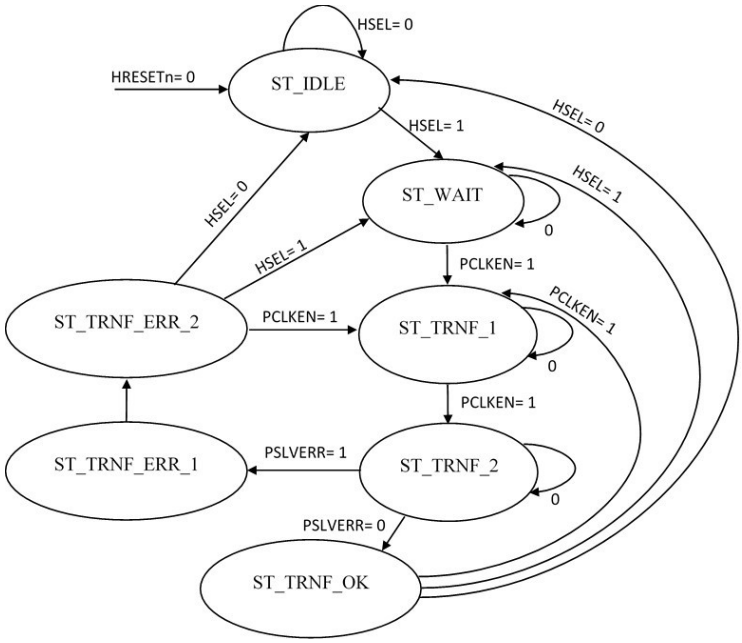

FIGURE 3. AMBA bridge FSM diagram.

TABLE 3. Power Consumption of Different Components for Various Tests.

Module	Bluetooth Transmit Test (mW)	Sleep Test (mW)	Timer Test (mW)	UART Test (mW)
Cortex-M0	1.128	1.064	1.140	1.130
WIC	0.055	0.055	0.055	0.055
SRAM	0.319	0.412	0.323	0.262
GPIO	0.268	0.259	0.265	0.261
UART	0.273	0.273	0.273	0.279
Watchdog	0.075	0.075	0.075	0.075
Timer	0.123	0.123	0.123	0.123
Dual timer	0.201	0.200	0.201	0.200
BLE	3.498	3.404	3.406	3.396
SPI	0.025	0.026	0.026	0.028
TDSP	0.036	0.036	0.036	0.036
RTC	0.117	0.117	0.117	0.117
Clock	21.755	21.755	21.755	21.755
Others	2.457	1.815	1.821	1.801
Total:	**30.330**	**29.613**	**29.616**	**29.517**

RESULT AND DISCUSSION

This work performs four power analysis tests: Bluetooth transmission, sleep, timer, and UART. The gate-level simulation results are shown in Table 3. From the table, the Bluetooth transmits test consumes the highest power (30.330 mW) compared with other tests. Due to the standby mode, Cortex-M0 consumes the least power during the sleep test compared to other tests. As expected, the UART module consumes the highest power during the UART

test, while the timer module's power consumption stays almost the same throughout all the power analyses. The clock network consumes around 70% of the power in all tests.

This paper applies clock gating to the design to improve power consumption. Next, Gray code state encoding is implemented on the system bridge. Table 2 shows the result of implementing the gated clock and the Gray code in the system. From the table, the clock network power consumption reduces by almost 99% compared to the design without the clock gating. The gated clock reduces most of the inactive module's flip-flops. The result shows that by implementing the clock gating, the power consumption of the processor decreased by 66%, SRAM 18%, GPIO 52%, UART 75%, watchdog 86%, timer 96%, dual timer 92%, Bluetooth 78%, SPI 79%, TDSP 84% and RTC 56%. This is equivalent to 84% power reduction for the whole system. The result of the system is further improved by implementing the Gray coding to the FSM of the bridge. The results show that power consumption on the buses and bridge components was reduced by 22 μW compared to binary state encoding. In total implementing

TABLE 4. Power Consumption for Gray Code State Encoding.

Module	Full Chip Integration	Full Chip Integration + Gated Clock	Full Chip Integration + Gated Clock + Gray Code
Cortex-M0	1.128	0.386	0.383
WIC	0.055	0.002	0.002
SRAM	0.319	0.265	0.260
GPIO	0.268	0.122	0.117
UART	0.273	0.069	0.069
Watchdog	0.075	0.011	0.011
Timer	0.123	0.005	0.005
Dual timer	0.201	0.017	0.017
BLE	3.498	0.778	0.772
SPI	0.025	0.004	0.004
TDSP	0.036	0.006	0.006
RTC	0.117	0.051	0.051
Clock	21.755	0.082	0.082
Buses	2.457	2.315	2.293
Total:	**30.330**	**4.113**	**4.071**

CONCLUSION

This paper analyzed the power consumption of a wireless Bluetooth microcontroller. The system has been synthesized using Silterra 180nm CMOS technology before being simulated at gate-level simulation using Synopsys System-on-Chip EDA Tools. Two low-power design methodology has been implemented: clock gating and Gray code encoding. Four power analysis tests have been performed to measure the switching activity: Bluetooth transmission, sleep, timer, and UART. The Bluetooth transmit test consumes the highest power among all the tests. Based on the simulation results, the clock gating reduces the overall system power consumption by 86%. In addition, the Gray code state encoding further reduces the system power consumption by 42 μW.

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REFERENCES

1. Bluetooth Special Interest Group, "From Prototype to Global Standard – Bluetooth Celebrates 20 Years of Market Creation," 2018. [Online]. Available: https://www.bluetooth.com/news/pressreleases/2018/01/from-prototype-to-global-standard-bluetooth-celebrates-20-years-of-market-creation. [Accessed: 10-May-2018].
2. K. Nair et al., "Optimizing power consumption in IoT based wireless sensor networks using Bluetooth Low Energy," in 2015 International Conference on Green Computing and Internet of Things (ICGCIoT), 2015, pp. 589–593.
3. C. Qiu, J. C. Xu, and S. C. Chen, "An ultra-low-power Bluetooth low-energy RF SoC with embedded flash and on-chip matching," in 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), 2019, pp. 1–3.
4. Y. K. Chen and S. Y. Kung, "Trend and challenge on System-on-a-Chip designs," J. VLSI Signal Process. Syst., vol. 53, no. 1–2, pp. 217–229, 2008.
5. Nordic Semiconductor, *nRF51822 Product Specification v3.1*, Trondheim, Norway, 2014.
6. T. Sanislav, S. Zeadally, G. D. Mois, and S. C. Folea, "Wireless energy harvesting: Empirical results and practical considerations for Internet of Things," J. Netw. Comput. Appl., vol. 121, pp. 149–158, 2018.
7. S. F. Gong and X. Q. Yin, "Solution of home security based on ARM and ZigBee," in International Symposium on Computer, Consumer and Control (IS3C), 2016, pp. 89–91.
8. A. Dementyev, S. Hodges, S. Taylor, and J. Smith, "Power consumption analysis of Bluetooth Low Energy, ZigBee and ANT sensor nodes in a cyclic sleep scenario," in IEEE International Wireless Symposium (IWS), 2013, pp. 31–34.
9. J. Hughes, J. Yan, and K. Soga, "Development of wireless sensor network using Bluetooth Low Energy (BLE) for construction noise monitoring," Int. J. Smart Sens. Intell. Syst., vol. 8, no. 2, pp. 1379–1405, 2015.
10. A. Pouraghily and T. Wolf, "A lightweight payment verification protocol for blockchain transactions on IoT devices," in International Conference on Computing, Networking and Communications (ICNC), 2019, pp. 617–623.
11. N. Mora et al., "IoT-based home monitoring: Supporting practitioners' assessment by behavioral analysis," Sensors (Switzerland), vol. 19, no. 14, p. 3238, 2019.
12. G. Mois, S. Folea, and T. Sanislav, "Analysis of three IoT-Based wireless sensors for environmental monitoring," IEEE Trans. Instrum. Meas., vol. 66, no. 8, pp. 2056–2064, 2017.
13. J. B. Kim, J. Woo Ahn, J. O. Kim, and S. Gon Choi, "A resource saving MAC/IP handling method for low-power wireless TCP packet network," in International Conference on Advanced Communication Technology (ICACT), 2019, pp. 196–200.
14. K. H. Dareen, C. M. Tang, M. S. Ng, and H. Dicky, "Software-based turbo decoder implementation on low power multi-processor System-on-Chip of Internet of Things," in 2017 4th International Conference on New Media Studies (CONMEDIA), 2017, pp. 137–141.
15. Y. Pu et al., "Blackghost: An ultra-low-power all-in-one 28nm CMOS SoC for Internet-of-Things," in 2017 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS), 2017, pp. 1–3.
16. N. H. E. Weste and D. M. Harris, *Integrated Circuit Design*, 4th ed. Boston: Pearson, 2011.
17. P. R. Panda, A. Shrivastava, B. V. N. Silpa, and K. Gummidipudi, *Power-efficient system design*, New York: Springer Science+Business Media, 2010.
18. X. Wang et al., "A multi-level collaboration low-power design based on embedded system," in 28th IEEE International System on Chip Conference (SOCC), 2015, pp. 186–190.
19. S. P. More and M. S. Borse, "Energy conservation in WSN using binary to gray topology," Int. Res. J. Eng. Technol., vol. 3, no. 5, pp. 1455–1458, 2016.
20. S. Heidari and E. Farzadnia, "A novel quantum LSB-based steganography method using the gray code for colored quantum images," Quantum Inf. Process., vol. 16, no. 10, pp. 1–28, 2017.
21. C. Qiu, F. Wu, C. Lee, and M. R. Yuce, "Self-powered control interface based on Gray code with hybrid triboelectric and photovoltaics energy harvesting for IoT smart home and access control applications," Nano Energy, vol. 70, no. December 2019, p. 104456, 2020.
22. V. Salauyou and L. Zabrocki, "Coding techniques in Verilog for Finite State Machine designs in FPGA," in IFIP International Conference on Computer Information Systems and Industrial Management (CISIM), 2019, vol. 11703, pp. 493–505.

23. W. T. Shiue, “Novel state minimization and state assignment in finite state machine design for low-power portable devices,” Integr. VLSI J., vol. 38, no. 4, pp. 549–570, 2005.
24. U. Berger, K. Miyamoto, H. Schwichtenberg, and H. Tsuiki, “Logic for Gray-code computation,” Concepts proof Math. Philos. Comput. Sci., vol. 6, p. 69, 2016.
25. T. Marconi, D. Theodoropoulos, K. Bertels, and G. Gaydadjiev, “A novel HDL coding style to reduce power consumption for reconfigurable devices,” in 2010 International Conference on Field-Programmable Technology (FPT), 2010, pp. 295–299.
26. R. Uma and P. Dhavachelvan, “Finite state machine optimization in FPGAs,” in Proceedings of the Second International Conference on Computational Science, Engineering and Information Technology (CCIEST), 2012, pp. 205–211.
27. A. Khalid, G. Paul, and A. Chattopadhyay, “Backgrounds,” in *Domain Specific High-Level Synthesis for Cryptographic Workloads*, Springer, Singapore, 2019, pp. 5–22.
28. M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, *Low power methodology manual for System-on-Chip design*, 1st ed. Springer Science & Business Media, 2007.
29. C. J. Lukas and B. H. Calhoun, “A 0.38 pj/bit 1.24 nW chip-to-chip serial link for ultra-low power systems,” in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 2860–2863.