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Design and Integrate Real Time Clock and Temperature Digital Signal Processing with ARM System

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Abstract. The integrated circuit had been developed rapidly from microprocessor to microcontroller and System-on-Chip (SoC) just happen within a few decade. The development is continuing as the demand for the functionality increase. The Real Time Clock (RTC) is one of the peripherals most widely used inside the microcontroller. Besides, when Moore's law is still applied, the number of transistor will increase, so does the temperature. Thus, the temperature digital signal processing (TDSP) unit had become an important peripheral to monitor the system-on-chip temperature. In this paper, these two Intellectual Property which are RTC and TDSP are designed and integrated into ARM system. The system architecture and implementation strategies are discussed. The results were run and simulated in the Synopsys software.

1. Introduction

The embedded system had evolve since it had been created. Since then, more and more transistor and function had been integrated together to accomplish the task. The system had already become the System-on-Chip (SoC), which all the peripherals are integrated into a single chip. The advantages of SoC are the overall performance and time to market compare to traditional Application Specific Integrated Circuits (ASIC) [1–3].

The most common component for a SoC is the Real Time Clock (RTC). It is widely used in many microcontroller or embedded system. For example, some of the devices need to record the real time when collecting the data [4]. The real time can provide the analyzer how the period of a particular data formed. The other common component that is widely used is the Temperature Digital Signal Processing (TDSP). It is needed when number of the transistors are increasing, and the temperature can be a disaster to the board [5]. The TDSP can prevent the processor and the peripheral overheat and cut off the power supply if necessary.

In this paper, two IP which are RTC and TDSP will be integrated into the ARM system. The ARM system include the Cortex-M0 core processor, the AMBA bus [6–8] and other ARM peripherals. The ARM system is readily to be use in order to reduce the time to market. The ARM system allow designer to modify, to suit the need. Some of the passed research also been review and compare in the following section. Design strategies are discuss in the methodology section. Result and discussion show the successful integration and verification using hardware software co-verification.

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2. Literature Review

In paper [9], a landmine system on chip detector was designed and implement on FPGA. The design was using AMBA bus architecture as the on chip bus to achieve a high speed processing. The system architecture made up of processor, concurrent processor, and some port as shown in Figure 1. The input data will be transfer from Digital Analogue Converter (DAC) in the processor. Then, the concurrent processor will process the signal. The result will be shown at the output port. This process will be repeated for the detection. A comparator inside the concurrent processor will compare the pre-stored value inside the memory.

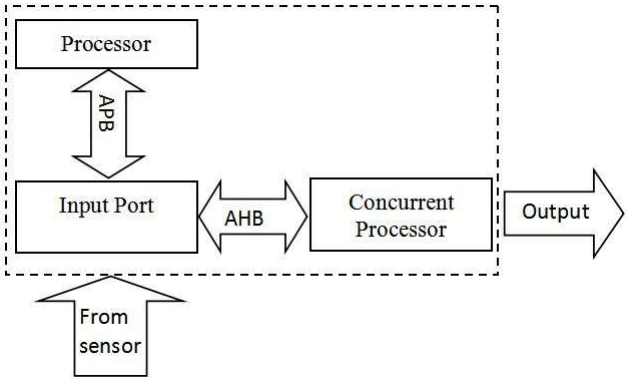

Figure 1. The block diagram of landmines architecture [9].

In paper [10], the author proposed a changeable processor platform in order to reduced time to market. The design include modules which are the building blocks for most of the embedded application such as timer, GPIO as shown in Figure 2. The design processor used in the design are ARM9 based processor and the PalmBus as the bus architecture. The CPU interface controller handle the signal between the processor and the PalmBus. The controller can decode up to 64MB address. The PalmBus will be receive either read or write request from the processor. The design was run on the Spartan3 and run with 33.3MHz. The design claim that only 19% FPGA slices is used and is suitable for more module using this platform.

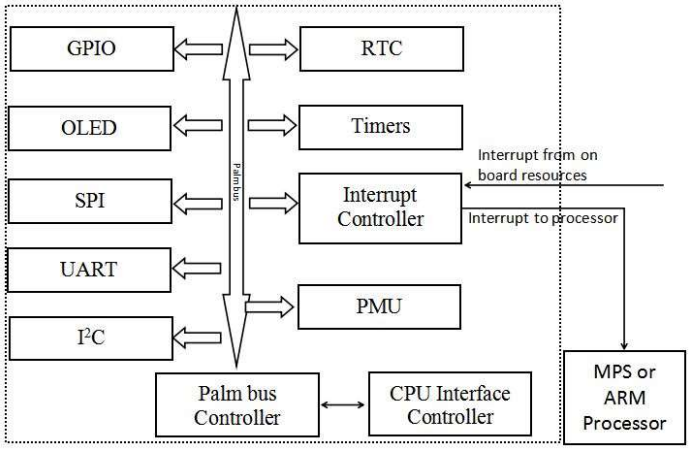

Figure 2. : The changeable processor architecture [10].

In paper [11], a power efficient x86 processor and an AMBA bus architecture system on chip was proposed. The PKUnity86 and an AMD Geode GX2 processor is design to support massive PC software resources such as Microsoft Window. The design was implement on Virtex-4 LX200 FPGA. The designer need to take care of address space, memory, I/O ad interrupt allocation, external float point unit exception, cache coherence that are huge difference between AMBA and the Windows system. The function of XAB component is to translate the transaction GeodeLink to AHB. The design was download into FPGA and run with Window XP BIOS.

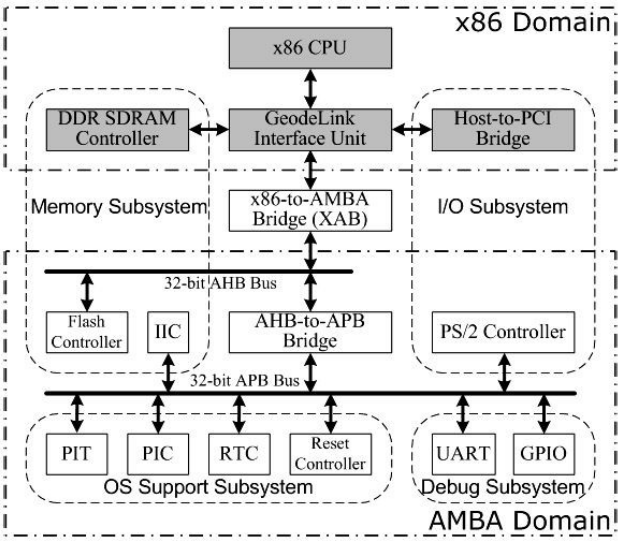

Figure 3. : The mixed x86 processor and AMBA architecture [11].

In paper [12], a AHB-DMA controller has been reviewed and shown in Figure 4. The Direct Memory Access (DMA) is the memory that is able to transfer the data from the bus and the IP directly for a given programmed count. Initially, the processor will start to program the operational registers of the AHB-DMA. The DMA will start to transfer data after receive the control word register and will generate interrupt after the process. The DMA enable to the processor away from transfer a long data.

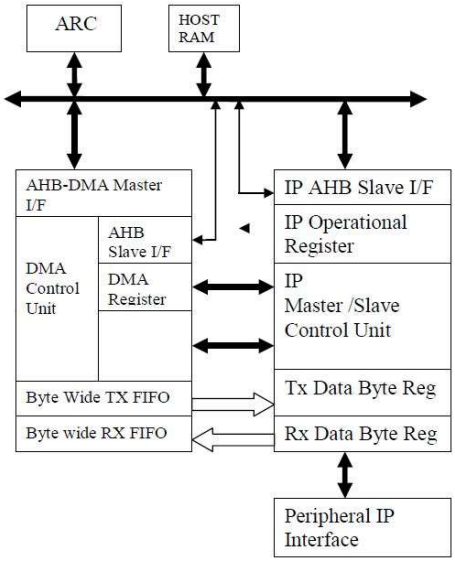

Figure 4. : The proposed DMA structure [12].

In paper [13], an APB controller and the peripheral devices had been integrated. The design architecture is based on the standard AMBA protocol. The design only focus on APB side and integrated with IP modules such as keypad decoder, timer, seven segment decoder, UART as shown in Figure 5. The AHB to APB Bridge is the master for the APB and the APB controller will control the flow of data and control signals. The design was implemented on the SPARTAN 3 board with 50MHz.

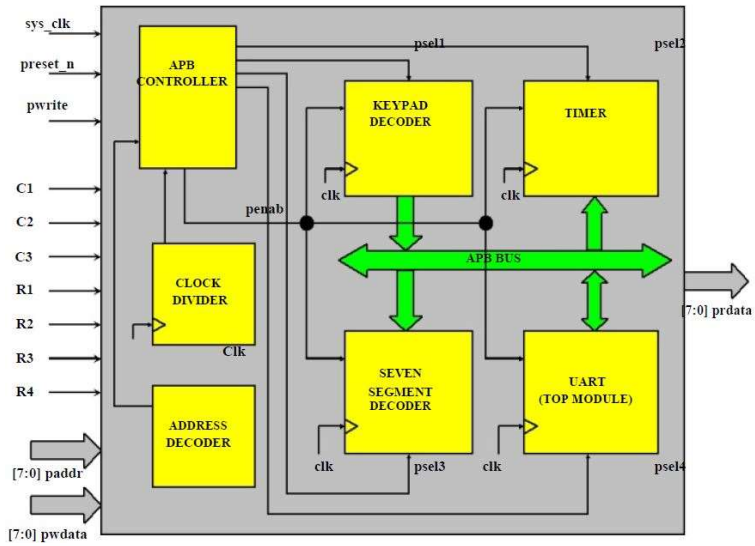

Figure 5. The APB controller on APB side [13].

In conclusion, several system architecture had been reviewed. Each of the design has its advantages, and challenges. Some the design had shown how to design and the way to implement on hardware which are useful for this paper.

3. Methodology

In this paper, the design start by using the ready to use ARM Cortex-M system design kit as the base system. The system include several peripheral such as AHB bus components, UART, GPIO. The design of two reusable IP are integrate into the system and create a multipurpose microcontroller. The design of RTC is include function controller, counter binary frequency divider and also an AMBA interface as shown in Figure 6 based on [14]. The RTC is consider the leap year feature, which the date will increase one day in every four years. Besides, alarm function also included in this IP. The counter resolution for this IP will up to plus minus 1 millisecond per counter. This will increase the accuracy of the clock.

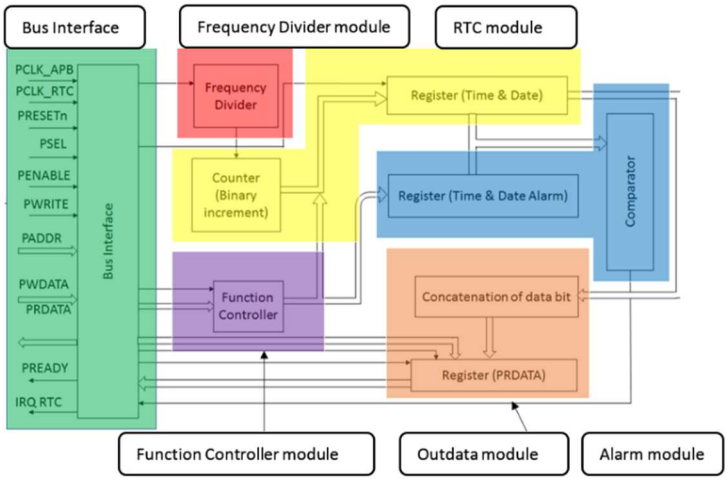

Figure 6. The design block diagram of RTC.

Next, Temperature Digital Signal Processing (TDSP) is design to monitor the temperature of the chip especially the part that has highly usage. The architecture in block diagram of TDSP is shown in Figure 7 based on [15]. The design also include AMBA bus protocol signal for reuse purposes. An interface register, function controller, programmable watchdog, and interrupt generator are the main components for this TDSP. The TDSP is able to give interrupt to the processor when the surrounding is overheat and

prevent hard fault on the chip. The conception of the TDSP is the processor will set a threshold value for the TDSP to compare the signal receive from Analogue Digital Converter (ADC). An interrupt will send out to the processor when the ADC value is higher than the threshold value.

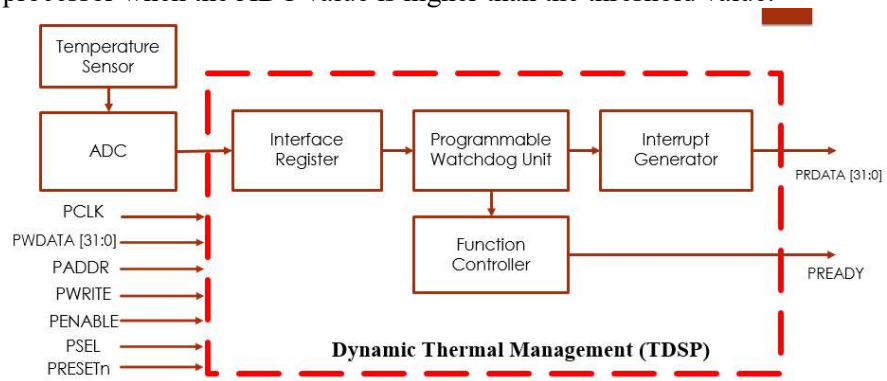

Figure 7. The block diagram for TDSP.

The overall system architecture is shown in Figure 8. All the IP are then integrated into the system with the memory map which is designed as shown in Table 1.

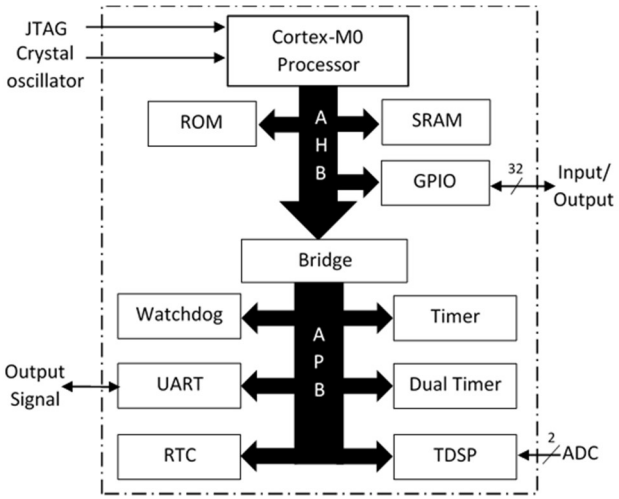

Figure 8. Overall system block diagram.

Table 1. Memory Map for the system.

Module	Base Address	End Address
ROM	0x0000_0000	0x0000_FFFF
RAM	0x2000_0000	0x2000_FFFF
Timer0	0x4000_0000	0x4000_0FFF
Timer1	0x4000_1000	0x4000_1FFF
Dualtimer	0x4000_2000	0x4000_2FFF
UART0	0x4000_4000	0x4000_4FFF
UART1	0x4000_5000	0x4000_5FFF
UART2	0x4000_6000	0x4000_6FFF
RTC	0x4000_7000	0x4000_7FFF
Watchdog	0x4000_8000	0x4000_8FFF
TDSP	0x4000_9000	0x4000_9FFF
GPIO0	0x4001_0000	0x4001_0FFF
GPIO1	0x4001_1000	0x4001_1FFF

Subsequently, an application for the processor is added. The program is generated using Keil software. The application use C language to test the design by input the time and date. The program let the RTC to run for a few cycle before other input. The alarm included by set a certain time to trigger the interrupt. Next, the TDSP is provided with the threshold value, and a model input from ADC was created in the testbench.

4. Result and Discussion

The Figure 9 show that the simulation waveform run in Synopsys. The important signal for the RTC was highlighted which are seconds, minutes, hours, date, months and years. The data 0x5096_9670 is transfer using write data bus which is known as PWDATA. The time shown is 08:18:52am and 21st June 2017. The design for date, month and years shown are not exactly the value as the time. This is because the design of RTC is initiate the value to zero and the software can adjust the value by plus one. The Figure 10 show the value input to TDSP. The TDSP show the interrupt when the value of ADC show high which the value from temperature sensor (INPUTADC) is 2'b11 and the interrupt is occurred in PRDATA which is 2'b10. The system and the support documents was obtained from ARM official website [14–15] through ARM University Program.

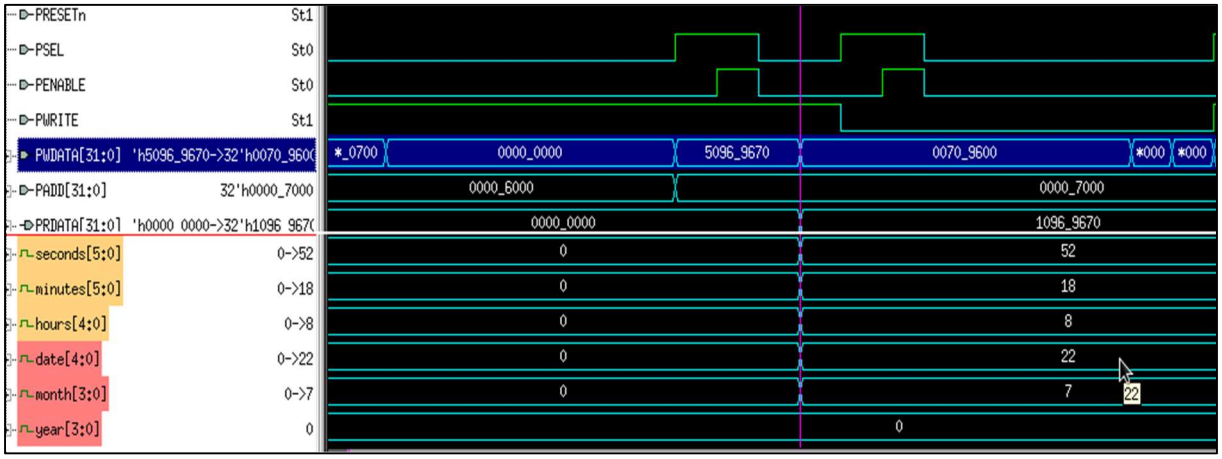

Figure 9. The test waveform of RTC.

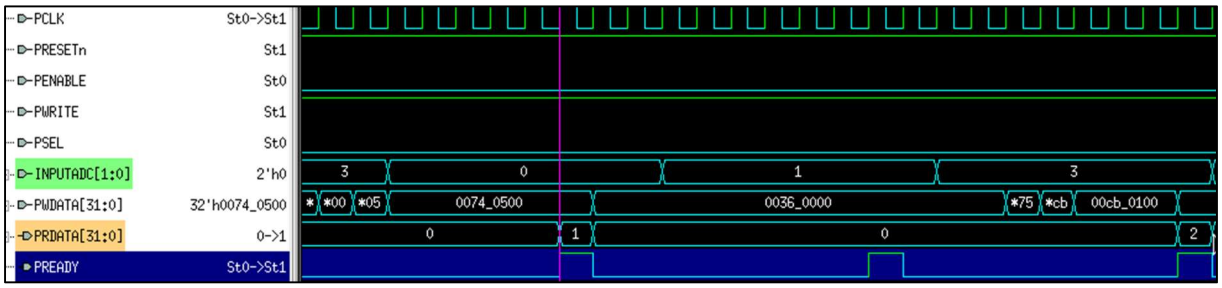

Figure 10. : The test waveform of TDSP.

5. Conclusion

This paper has presented the design of a system on chip microcontroller system. The primary goal of this effort is to design the reusable IP and integrate into the AMBA platform. The most widely used IP such as RTC and TDSP are chosen as the IP to integrate. The result was run on Synopsys tool and the simulation result showed was same as intended. In future study, more and more IP can be design and integrate into this microcontroller so that the microcontroller is multi-function.

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