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Analysis of Microprocessor System Interface with Memory

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***Abstract*—The microprocessor is one of the digital components that is widely used in the market todays. Soft-core microprocessors have been widely used in embedded systems. The soft-core processor has become the target of interest for researchers. In this paper, several soft-core processor architectures and systems are reviewed. Then, the analysis of microprocessor system's interface with memory is carried out. Detailed read and write operations on the memory are discussed and compared with theory. The experiment was carried out by loading the microprocessor system architecture into Altera Cyclone II field programmable gate array (FPGA). The experimental results show that the read and write operations on the memory succeeded. The total power estimation is 203.67mW.**

***Keywords*—microprocessor, soft-core processor, SDRAM, memory**

I. INTRODUCTION

Microprocessors have been in use since decades ago. Early microprocessors operated using 4 bit or 8 bit, as used in calculators. At present, the microprocessor has evolved into a powerful computing tool and is used in commercial products such as computers, where it is integrated with other components such as memory, peripherals and data buses to become an embedded system or system-on-chip (SoC). Some examples of applications are smartphones, digital cameras and automobile systems.

One of the approaches to developing an embedded system is to implement it into field programmable gate array (FPGA). FPGA is an integrated circuit (IC) that contains arrays of configurable logic block connected with configurable interconnects where it can be reprogrammed by a designer [1]. In this approach, an embedded system is designed in a hardware description language (HDL) such as Verilog HDL or Very High Speed Integrated Circuit (VHSIC) HDL (VHDL). HDL contains information about the structure, design and operation of electronic circuits for applications or systems. The FPGA is programmed with HDL to become an embedded system.

A soft-core processor is required to design an embedded system in FPGA. It is a processor that is described in HDL or a logic circuit and implemented in FPGA or application specific integrated circuit (ASIC) via logic synthesis [1]. Examples of soft-core processor are Nios II from Altera and MicroBlaze from Xilinx. The flexibility of the soft-core processor allows it to be widely used in FPGA since it can be customized for specific applications.

In this paper, a microprocessor system with memory is implemented and analysed in FPGA. Section II discusses several existing microprocessor architectures, while section III presents the methodology for implementing the microprocessor system in our work. In section IV, the experimental results of the microprocessor system's interface with memory are discussed. Finally, section V concludes this paper.

II. LITERATURE REVIEW

In paper [1], a multiprocessor system on chip based on the programmable processor core Nios II Altera is developed and analysed. The multiprocessor system contains three Nios II processor cores connected with a timer core and 4KB of instruction cache. A total of 10,785 logic elements and 27 KB internal memory is used. The microprocessor system is designed and synthesized using system on programmable chip (SOPC) software. The microprocessor system module produced from the software is connected to an I/O circuit contact in Quartus II software, as illustrated in Fig. 1. The design file is loaded to FPGA Cyclone II EP2C35F672C6 in an Altera Development and Education 2 (DE2) board. Nios II Software Build Tools for Eclipse are used to initialize and program the processor. The test result is previewed through the console window of NIOS II software.

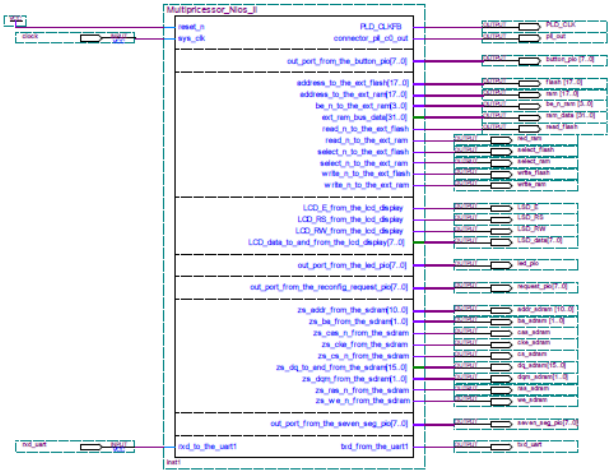

Fig. 1. Structural module in Quartus II CAD [1]

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In paper [2], a 16-bit microprocessor architecture is designed and simulated on FPGA using VHDL. The processor uses a 16-bit reduced instruction set computing (RISC) microprocessor. A 64 KB memory is interfaced with the central processing unit (CPU) and the proposed design is tested with application programs that execute memory-related operations. The block modules illustrated in Fig. 2 represent the processor and the memory where the arrow line represents the interconnection. The memory component contains the instructions and data for the processor to execute. Xilinx software is used for synthesis and simulation of the processor. The synthesized design will be loaded to a Spartan FPGA device for testing. The analysis of maximum delay operation and fan out is carried out. A total of 260 Flip Flops and 335 lookup tables (LUT) are used for the design.

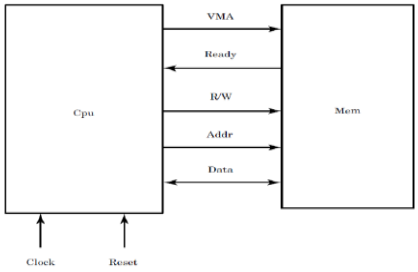

Fig. 2. Hardware representation of 16-bit microprocessor [2]

The author of [3] presents the design of an 8-bit RISC microcontroller in FPGA. The microcontroller architecture is based on Microchip PIC16 microcontrollers. The author claims that the proposed architecture is four times faster than the original Microchip PIC16 architecture under the same clock at the same frequency. In paper [3], four different microcontroller instruction cycle structures have been tested, and the results show that the proposed designs are faster than the Microchip PIC16 microcontroller. The downloader module was proposed to direct the data to the program memory using a generic serial interface. The block diagram and interconnection of the system are illustrated in Fig. 3.

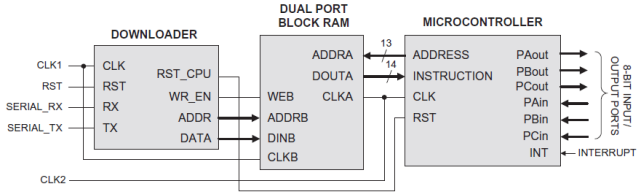

Fig. 3. Block diagram of the proposed microcontroller system [3]

In paper [4], a multicore single program, multiple data architecture is proposed to compute data-intensive signal processing applications. The multicore architecture is designed based on a replication design methodology. A Nios II processor is selected as a processor for multicore architecture along with an Avalon bus for interconnection. Four core architectures are illustrated in Fig. 4. Three different algorithms are used to test the architecture which are FIR filter, spatial Laplacian filter, and matrix-matrix multiplication. From the results, execution time is shortened when the number of cores increase at the expense of parallel efficiency.

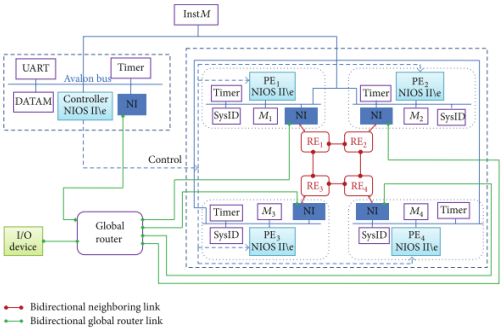

Fig. 4. Four core architecture [4]

The author in [5] proposed a new open source RISC processor, SecretBlaze. SecretBlaze is a MicroBlaze instruction set compliant processor. It use a different data path as illustrated in Figure 5, which provide instruction level parallelism with a five-stage pipeline. The memory sub-system for SecretBlaze illustrated in Fig. 6 is responsible for organizing the memory and I/O devices. Wishbone buses are also in used in this architecture. The design is synthesized and successfully tested on a Digilent Xilinx Spartan-3 Starter Kit Board with a low-cost XC3S1000 FPGA.

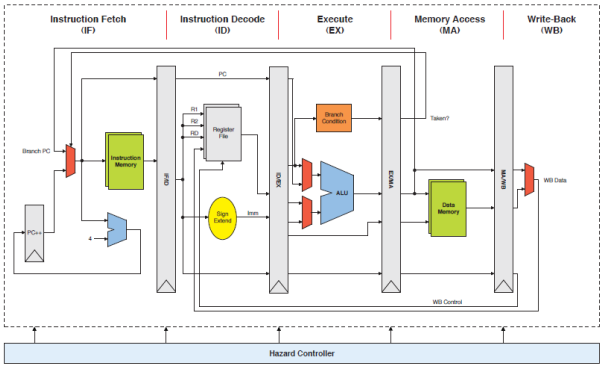

Fig. 5. SecretBlaze data path [5]

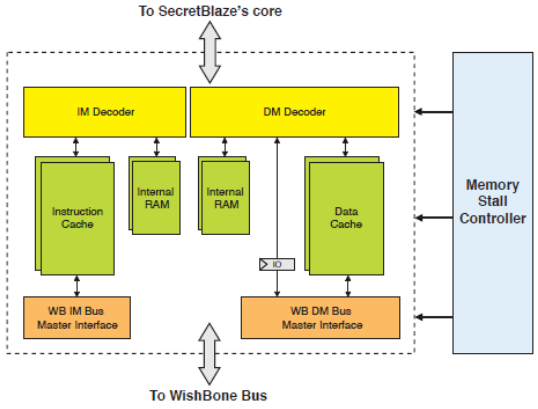

Fig. 6. SecretBlaze memory sub-system [5]

A comparison of several soft-core processor architectures is made and tabulated in Table I. Based on

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Table I, 8-bit, 16-bit and 32-bit processors are popular in researching soft-core processors. A soft-core processor can be used to design a multiprocessor system, as in [1] and [4]. The memory component used in the architecture is dependent on user and design need. Xilinx software such as Xilinx ISE and Altera software such as Quartus II and ModelSim are widely used in the design and synthesis of the architecture. Verilog and VHDL are the most common HDL languages used to design the architectures. Several types of FPGA chip are used in implementing microprocessor systems, such as Spartan 3, Startix V and Cyclone II. The logic block size is dependent on the microprocessor structure, multi core system, and selected FPGA chip.

Table I. Comparison between different processor architectures

Architecture	[1]	[2]	[3]	[4]	[5]
Processor	Altera Nios II	16-bit custom processor	8-bit PIC16F87 based uc	Altera Nios II	MicroBlaze processor based
Multi core	YES	NO	NO	YES	NO
Memory	27Kb internal Mem.	64KB	192B	8KB prog. Mem., 3KB Data Mem.	4GB accessible address 32-bit memory
Software	Altera	Xilinx	Xilinx	Altera	Xilinx
FPGA	Cyclone II	-	Spartan 3A	Startix V	Sparta 3
Logic Block	10,785 logic elements	216 slice	317 – 530 slice	3905 LUT	1179 LUT
HDL	-	VHDL	Verilog	-	VHDL

In this paper, a microprocessor system is proposed to interface with a memory component. Altera Nios II processor is used as the main processor core. Synchronous dynamic random access memory (SDRAM) is used as a memory component. An analysis of the microprocessor system's interfacing with memory is made through read and write operation on SDRAM.

III. METHODOLOGY

In this section, the methodology for a simple microprocessor system interfaced with memory will be explained. The proposed microprocessor system contains a Nios II processor, general input and output (GPIO), on-chip memory, SDRAM with SDRAM controller, Joint Test Action Group (JTAG) universal asynchronous receiver transmitter (UART) and Avalon buses. The block diagram of the microprocessor system is illustrated in Fig. 7. For this microprocessor system, Nios II economy version processor is used. Nios II processor economy version is a 32-bits general purpose RISC processor with a minimal core size [6]. The processor core has less than 7,000 logic elements and able to perform over 30 Dhrystone million instructions per second (DMIPS) at up to 200 MHz of clock frequency [6].

The microprocessor system is created using the Qsys tool from Quartus II software. The system components such as Nios II processor, I/O core, SDRAM controller, on-chip memory and JTAG UART core are integrated to form a system using Qsys. Qsys is used to specify the components required by the system. The interconnection of components in the system is automatically generated by Qsys. The microprocessor system is synthesized by Qsys to generate a design file. Quartus II software provides the I/O circuit contact to the microprocessor system architecture. The microprocessor system architecture is downloaded to Cyclone II EP2C70F896C6 FGPA chip in the Altera DE2 board.

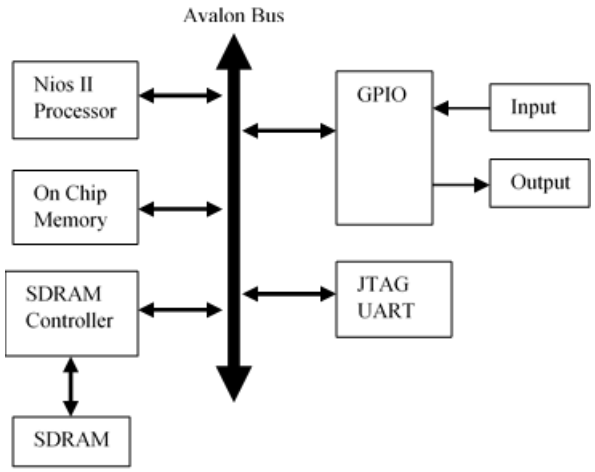

Fig. 7. Block diagram of proposed microprocessor system

In order to program the processor, Nios II Software Build Tool for Eclipse is used as a chain tool platform for Nios II processor system. Nios II Software Build Tool for Eclipse allows for the compilation of programming code, downloading of compiled Hex code to the microprocessor system and also the simulation for the microprocessor system in ModelSim software. In this research, the microprocessor system is analysed using simulation and FPGA hardware. In testing and analysing the system, a simple memory read and memory write on the SDRAM application code is used as a test code for the microprocessor system where the code is downloaded into the chip memory.

IV. RESULTS AND DISCUSSION

The microprocessor system is designed, integrated and synthesized in Quartus II software and Qsys software. The compilation of the design is based on the Cyclone II device family, device model EP2C70F896C6. Based on the compilation report, a total of 2,695 logic elements are used. The system is programmed with the Nios Software Build Tools, a tool chain for the Nios II processor. It is programmed to carry out a write operation on 32Mbyte

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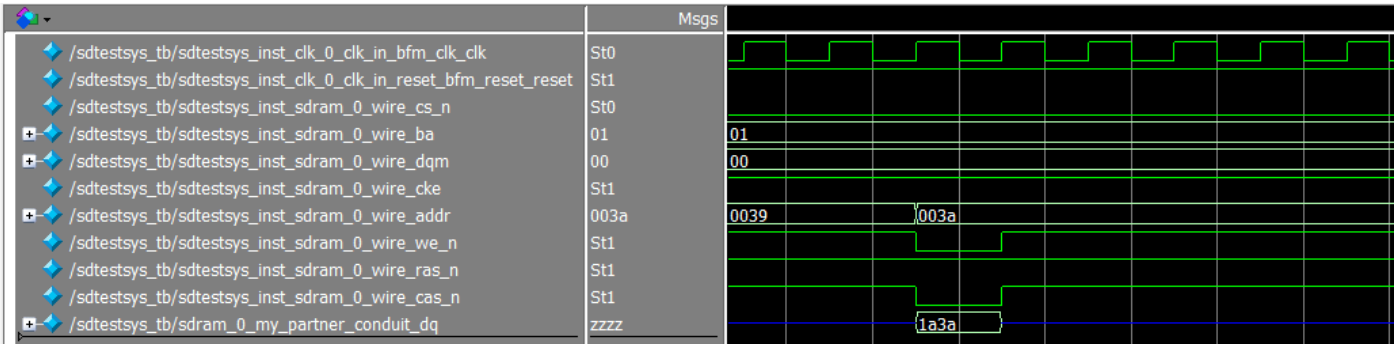

Fig. 8. Waveform diagram for SDRAM write operation

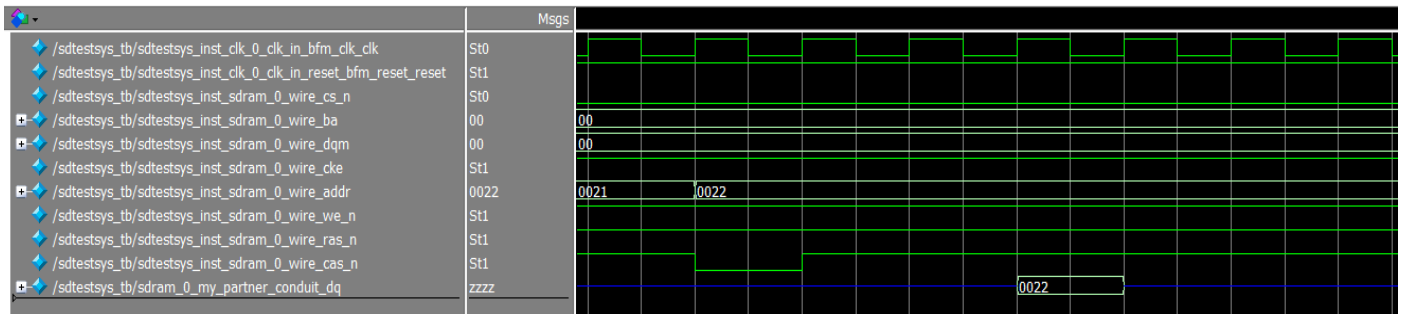

Fig. 9. Waveform diagram for SDRAM read operation

SDRAM and then a read operation on 32Mbyte SDRAM for all the addresses.

The microprocessor system is simulated using ModelSim software where the signal involved in the read and write operation on SDRAM is observed and analysed. The simulation results are observed in the waveform diagram as illustrated in Fig. 8 and Fig. 9. Based on the simulation results, the microprocessor interfacing with SDRAM required specific inputs and outputs which are chip select (cs_n), bank select (ba), data input/output mask (dqm), clock enable (cke), address bus (addr), write enable (we_n), row address strobe command (ras_n), data bus(dq), and column address strobe command (cas_n). Chip select is set to low while clock enable is set to high because only one SDRAM is used in the system.

During write and read operation, row address strobe command is set to high and column address strobe command is set to low. Fig. 8 shows the signal flow of the write operation on the address of 0x003A in the SDRAM. During write operation, the write enable signal is set to low. The address bus is loaded with the address value and the data bus is also loaded with the data value. Fig. 9 illustrates the waveform diagram for the signal flow of the read operation on address 0x0022 in SDRAM. During read operation, write enable is kept high and the address bus is loaded with the address value. The data bus maintains high impedance for the three clock cycle after the write enable and address bus are set. Then, the data bus is output with the value of data stored at the selected address location in SDRAM. Based on the read and write operation, row address strobe command, column address strobe command, write enable and data bus are set to the initial state after a single clock pulse. Comparing the simulation result with the datasheet, the simulated results can be seen to match the signal flow characteristic of the datasheet [7].

To test the microprocessor system in FPGA hardware, the architecture is loaded into the Cyclone II EP2C70F896C6 FGPA chip in Altera DE2 board using Quartus II software and Altera USB Blaster programmer. The application program code is compiled into Hex code using Nios II software. The Hex code is downloaded into the processor and allowed to execute the program. The program provides instructions to the processor to perform the write operation to all the registers in SDRAM with 16 bits of data. Then, the program provides instructions to the processor to perform the read operation on all registers in SDRAM and compare the data value from the write operation and the read operation on SDRAM. A total of 16777215 iterations of the write and read operation are carried out by the processor in order to access all the registers in SDRAM. Each read and write operation is carried out with 16 bits of data. Different values of data are inserted into SDRAM through the write operation. The data values used in the read and write operation and the number of errors for each type of data are listed in Table II.

The number of unmatched data values between the write and read operation is stored in the internal memory of the system and is output by a system peripheral such as UART port. The console window illustrated in Fig. 10 is the communication output between the PC and the microprocessor system through a JTAG UART. The console window indicates the progress of the application and also the number of errors occurring during reading and comparing the SDRAM value. Based on the writing and reading of the microprocessor

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system on the FPGA, the results show no errors in writing or reading memory.

Table II. Data value for read and write operation and number of errors

No.	Data value	Number of errors
1	Repeat of increment value from 0x0000 to 0xFFFF	0
2	Toggle data between value 1111 1111 1111 1111b and value 0000 0000 0000 0000b	0
3	Toggle data between value 1010 1010 1010 1010b and value 0101 0101 0101 0101b	0

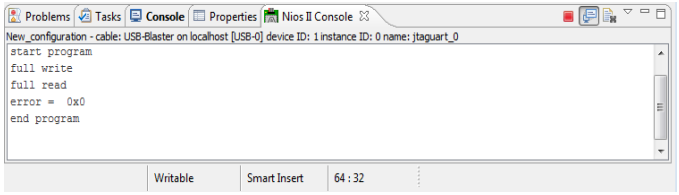

Fig. 10. Console window for communication between PC and microprocessor system

According to the PowerPlay Analyser tool in Quartus II, the total reported thermal power dissipation is 203.67 mW. The core static power dissipation is 154.98 mW and the I/O thermal power dissipation is 45.95 mW. The measurement output is based on the vectorless estimation toggle rate.

The proposed system is designed for the purpose of analysing the read and write operation on an SDRAM by the Nios II processor. The advantage of the proposed system is that it allows user to design the system more simply by using the Qsys tool from Quartus II software and intellectual property (IP) cores provided by Altera in Quartus II software. In the future, the proposed system be will further improved into an application-based microprocessor system, such as a data acquisition system or sensor-based system.

V. CONCLUSION

In this paper, the implementation of a microprocessor system interfacing with memory is carried out and the system is observed and analysed. Several existing microprocessor architectures and systems are also discussed. In this work, a microprocessor system utilizing a Nios II soft-core processor is designed, synthesized, programmed and simulated using Quartus II, Nios II Software Build Tools and ModelSim-Altera software. The simulation results from ModelSim-Altera software match the signal flow of the read and write operation on SDRAM as given in the datasheet. The microprocessor system has been implemented in Cyclone II FPGA hardware to test the interfacing between microprocessor system and SDRAM. From the experiment, the system is able to perform the read and write operation for all the SDRAM addresses successfully, with a power estimation of 203.67 mW.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

[1] K. Iryna and A. Storozhuk, “Multiprocessor System on Chip based on programmable processor cores Nios II Altera,” in *COMPUTER SCIENCE & ENGINEERING 2013*, 2013, no. November, pp. 32–33.

[2] N. Gupta, P. Gupta, H. Bajpai, R. Singh, and S. Saxena, “Analysis of 16 Bit Microprocessor Architecture on FPGA Using VHDL,” *Int. J. Adv. Res. Electr. Electron. Instrum. Eng.*, vol. 3, no. 4, pp. 8979–8986, 2014.

[3] Z. Hajduk, “An FPGA embedded microcontroller,” *Microprocess. Microsyst.*, vol. 38, no. 1, pp. 1–8, 2014.

[4] M. Baklouti and M. Abid, “Multi-Softcore Architecture on FPGA,” *Int. J. Reconfigurable Comput.*, vol. 2014, pp. 1–13, 2014.

[5] L. Barthe, L. V. Cargnini, P. Benoit, and L. Torres, “The SecretBlaze: A configurable and cost-effective open-source soft-core processor,” in *IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum*, 2011, pp. 310–313.

[6] *Nios II Processor Reference Handbook*. Altera Corporation, 2014.

[7] “256-MBIT SYNCHRONOUS DRAM,” *IS42S83200B datasheet*, Integrated Silicon Solution, Inc., 2007.

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