CHAPTER 9

A Study of an Interfacing Microprocessor System with Audio Codec Using an Altera DE2-70 Board

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9.1 Introduction

Audio codec is an integrated circuit that encodes analogue audio signal as a digital signal and decodes the digital signal into the analogue signal. Basically, it is an audio data converter that contains an analogue-to-digital converter (ADC) and a digital-to-analogue converter (DAC). The ADC and the DAC technology can be different with different audio codecs, such as successive approximation ADC and delta-sigma ADC [1]. The sensitivity of the audio codec also depends on the bit number of the ADC and the circuit inside the audio codec.

Interfacing with an audio codec depends on the communication protocol, for example inter-integrated circuit (I2C) or serial peripheral interface (SPI) [2]. A microprocessor system requires a communication module or driver to interface with an audio codec. The module will help to improve data transfer and connectivity between the microprocessor and the audio codec. This allows the microprocessor system to suffer fewer general-purpose input/output (GPIO) and interface compatibility issues when interfacing with an audio codec.

An audio codec can be applied in many applications by integrating it in different types of platform, such as a digital signal processor (DSP) system, a microprocessor system, system on a chip (SoC) or computer system [2]-[8]. Most applications that implement an audio codec are in the audio industry, such as smartphones, portable media players and audio systems [5]-[7]. However, it also applied in other industries, such as in electronic stethoscopes and speech recognition [3], [4], [8].

In this chapter, a microprocessor system with audio codec is implemented and analysed using field programmable gate array (FPGA). Section 9.2 discusses several existing microprocessor architectures for audio application, while section 9.3 presents the methodology for implementing the microprocessor system in our work. In section 9.4, the experimental results for the microprocessor system interface with audio codec are discussed. Finally, section 9.5 concludes this chapter.

9.2 Literature review

A microprocessor system for audio application is proposed by the author of paper [5]. The microprocessor system contains a Nios II processor, SD card controller, SPI communication module, audio codec driver, GPIO and other peripherals. The system architecture is downloaded into a DE2 board for demonstration. A Wolfson Wm8731 audio codec and SD card interface with the system. The system is able to play, pause and reverse-play music at different speeds using wave files stored in the SD card. It is able to record sound. The system architecture is

implemented using the SOPC Builder tool and Nios II Eclipse software. The setup of the project is illustrated in Figure 9.1.

Figure 9.1: Project setup including speakers, mic and DE2 board connected to the computer [5]

In paper [7], a digital voice recording system is introduced. The system architecture is illustrated in Figure 9.2, and consists of a Nios II processor, Avalon busses module, peripheral input/output (PIO), synchronous dynamic random access memory (SDRAM) controller, direct memory access (DMA) controller, I2C module, and audio data buffer module. The system design is tested on an experimental board with Altera's Cyclone II Series EP2C35 FPGA chip together with a Wolfson Wm8731 audio codec and SDRAM. The system architecture is designed using an SOPC Builder tool and Altera's IDE software development tools. Based on the test results for the system, the system can operate at 20 MHz with 16 bit high-speed audio data acquisition.

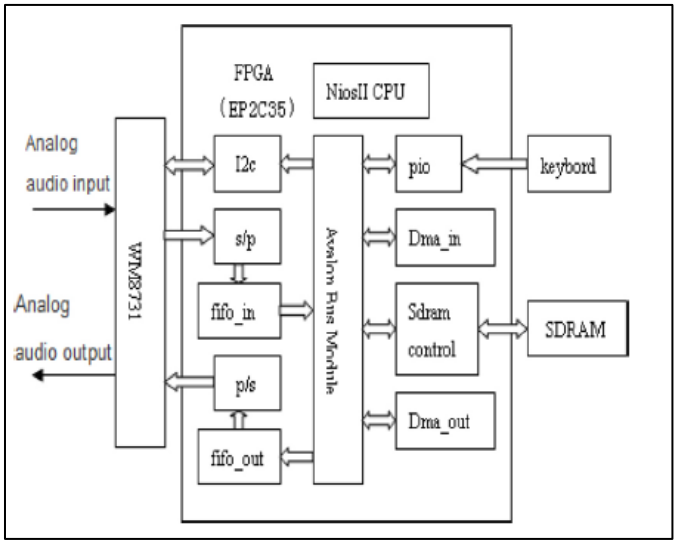

Figure 9.2: Schematic structure of the system hardware [7]

In audio applications, speech recognition is one of the interesting topics of research. A voice signal processing system based on DSP and FPGA is introduced by the author in paper [8]. The system is divided into four major modules, which are DSP minimum system module, external memory module, audio module and communication with host module. The DSP

minimum system module is the main processor for the system, where it is used to execute algorithm signal processing. The external memory module is a memory system that interconnects between DSP and external memory, for example FLASH, SDRAM or static random access memory (SRAM). The audio module is an audio driver that interfaces between the DSP and a Texas Instruments AIC23 stereo audio codec. The audio module contains an SPI controller for configuration on the audio codec and a buffer to transfer data between the audio codec and the DSP. Communication with the host module provides UART communication between DSP and PC and also enables online debugging of the system. The block diagram for the overall system is illustrated in Figure 9.3. The system is able to execute three functions, which are voice signal input, voice signal output and voice signal processing. The voice signal input and output are controlled by FGPA, and the signal processing takes place in the DSP. The system is tested with a speech recognition algorithm and the results show a high success rate in recognizing voice by the system.

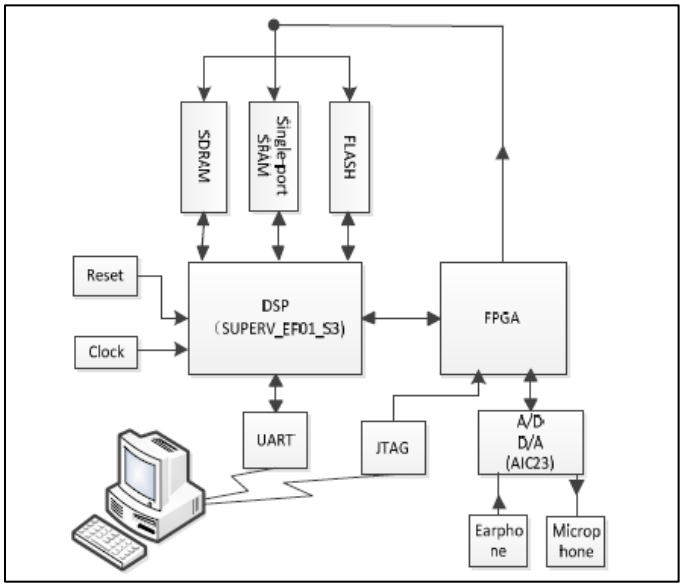

Figure 9.3: Block diagram of overall system [8]

An advanced microcontroller bus architecture (AMBA) based SoC for real-time audio processing is introduced in paper [6]. In the system, an audio coprocessor is designed to provide the SoC solution for real-time audio application. The proposed system contains a LEON 3 processor, AMBA bus, SDRAM with SDRAM controller, DMA module and audio module. The audio module consists of an audio codec driver, input buffer, output buffer, Hann window and 256-point FFT/IFFT (fast Fourier transform/inverse fast Fourier transform). The system block diagram is illustrated in Figure 9.4. The audio module is specifically designed for the Wolfson Wm8731 audio codec. The SoC design is implemented in the Altera DE2-115 board for testing purposes. An experiment is carried out on the FPGA board to analyse the FFT and IFFT processes with and without a Hann window application. The results show that the application of the Hann window has improved performances and reduced noise.

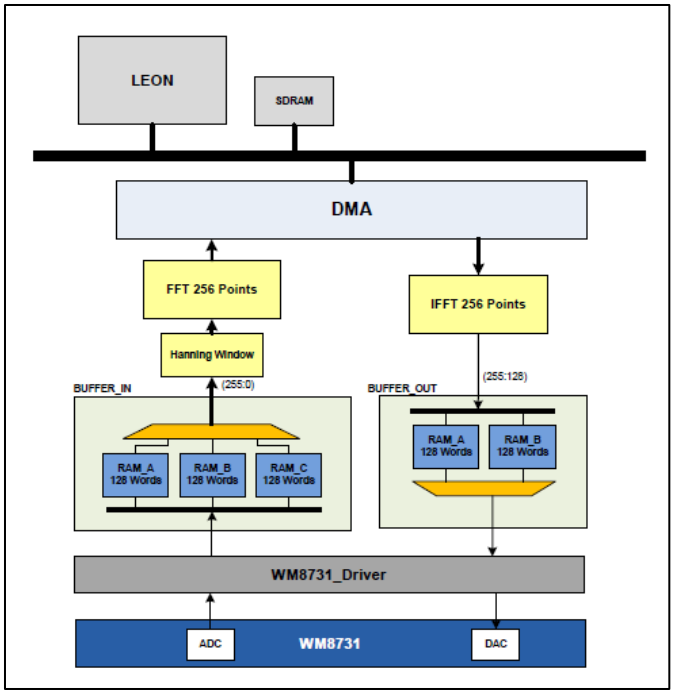

Figure 9.4: Audio coprocessor architecture [6]

In paper [4], an electronic stethoscope using FPGA with a real-time heart sound de-noising feature is constructed. The proposed system is capable of filtering out heart sound from the real-time captured lung sound. An adaptive line enhancer (ALE) filter was selected as a heart noise reduction method and the filter structure is implemented in the system. The proposed system consists of three parts, which are the DE2-70 development board, the audio codec with audio codec controller and pre-amplifier, and the anti-aliasing filter. The audio codec controller is designed for WM8731 audio codec. The block diagram of the proposed system is illustrated in Figure 9.5. An experiment is carried out using a heart sound mixed with a wheezing breath sound, and a heart sound mixed with a breath sound with crackles. It showed that the proposed system is able to reduce heart sound noise.

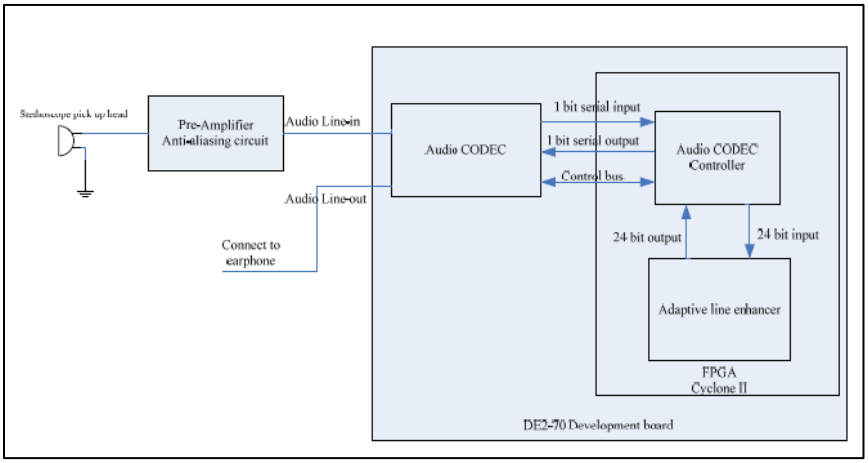

Figure 9.5: Block diagram of proposed system [4]

The differences between the existing microprocessor systems for audio application are tabulated in Table 9.1. The systems are able to perform audio player, speech recognition and audio signal processing tasks. Based on Table 9.1, various types of microprocessor are used in the microprocessor system, such as Altera Nios II processor, DSP and LEON 3 processor. Most of the systems used SDRAM to store program code and also audio data. However, some of the systems used other forms of external memory for data storage, such as SD card, FLASH and SRAM. Among the systems, Wolfson WM8731 audio codec is widely used by the researchers. Texas Instruments AIC23 stereo audio codec is used in one of the systems. Altera's Quartus II software and Altera's DE2 education board are used by most researchers as they are conventional, and easy to build and test. The SOPC Builder tool from Quartus II software is used by researchers because it can integrate systems easily.

Table 9.1 Comparison between different audio systems

	[5]	[7]	[8]	[6]	[4]
Processor	Altera Nios II	Altera Nios II	DSP	LEON 3	-
Memory	SD card	SDRAM	FLASH, SDRAM, SRAM	SDRAM	-
Software	Quartus with SOPC	Quartus with SOPC	Quartus	Quartus	Quartus
Audio codec IC	Wolfson WM8731	Wolfson WM8731	Texas Instruments AIC23	Wolfson WM8731	Wolfson WM8731
Hardware	DE2-35 board	DE2-35 board	Custom board	DE2-115 board	DE2-70 board
Application	Audio player	Audio player	Speech recognition	Audio signal processing	Audio signal processing

In this chapter, a microprocessor system is proposed to interface with an audio codec. An experiment is carried out to test the functionality of the microprocessor system and audio codec. An analysis is carried out on the input and output signal from and to the audio codec that is interfaced with the microprocessor system.

9.3 Methodology

In this section, the methodology of a microprocessor system interfaced with an audio codec, Wolfson WM8731L, will be explained. The microprocessor system architecture is designed, synthesized and programmed using Quartus II software and Nios II Software Build Tool (SBT). The system architecture is created using Qsys tool in Quartus II software. Qsys tool is a system integration tool that interconnects subsystems such as processors, busses and memory into a system. It also synthesized a system and generated its design file. In Quartus II software, the input and output (I/O) of the architecture can be linked to the I/O circuit in FPGA. Quartus II

programming software is used to load the system architecture into the Cyclone II EP2C70F896C7 FGPA chip in the Altera DE2-70 board.

The block diagram of the proposed microprocessor system is illustrated in Figure 9.6. In order to interface with the audio codec, Wolfson WM8731L [9], an I2C communication module and audio buffer module are required. The I2C communication module is used to initialize and alter the operation mode of the audio codec, while the audio buffer module is a data buffer to receive and send data to and from the audio codec. With this requirement, the proposed microprocessor system contains a Nios II processor, on-chip memory, 32 MB SDRAM with SDRAM controller, Avalon busses, a Joint Test Action Group (JTAG) universal asynchronous receiver transmitter (UART), I2C communication module and audio buffer module. Nios II economy version processor is used in the microprocessor systems.

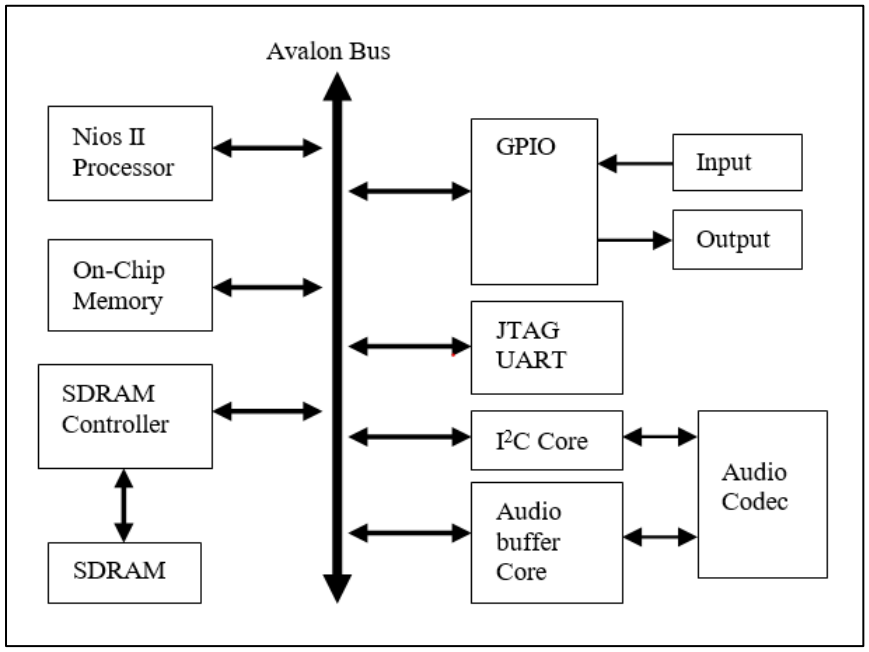

Figure 9.6: Block diagram of proposed microprocessor system

The interconnection of system components in Qsys tool software is illustrated in Figure 9.7. The system components are two clock sources, clock module, on-chip memory module, Nios II processor module, two SDRAM controller modules, Joint Test Action Group universal asynchronous receiver/transmitter (JTAG UART) module, audio configuration module, audio buffer module and peripheral input/output. Both clock sources are connected to the clock module. The clock module alters the clock frequency and provides it to the other module. The clock module also generates an external clock signal for SDRAM and the audio module, where SDRAM is operated at a frequency of 50 MHz with -0.3 ns phase-shifted clock signal, and the audio module uses 12.88 MHz frequency clock signal for data transfer. The data bus and instruction bus of the Nios II processor module are connected to on-chip memory and SDRAM, while the other module is connected to the data bus only.

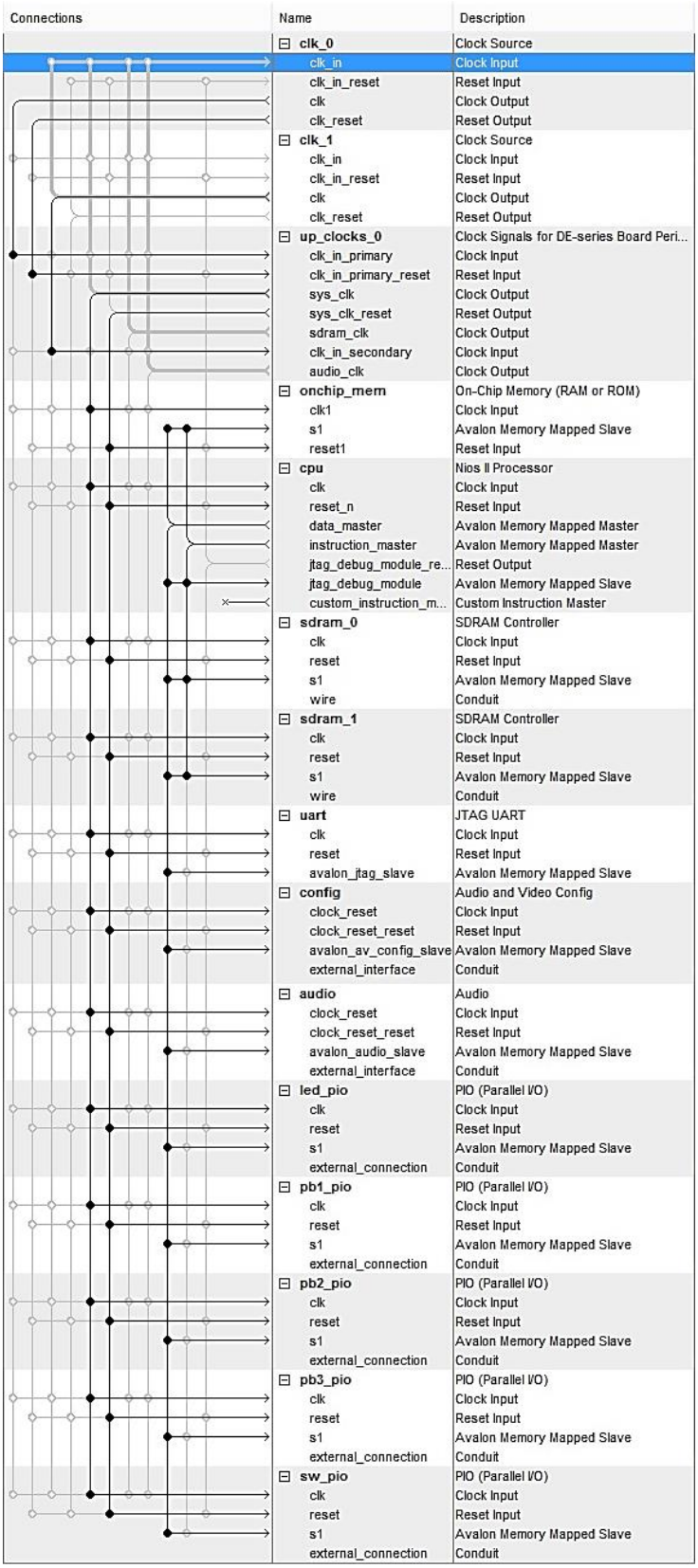

Figure 9.7: Interconnection of system components in Qsys

In this work, a program is coded and programmed to the system to allow the processor to carry out two different tasks. First, it receives input data from the audio codec then stores it in the memory. The second task is to retrieve the data from the memory then output the data in a form of signal through the audio codec. This program is used to validate the functionality of the system interfaced with the audio codec. Nios II SBT is used to program the Nios II processor system. Three different signals are used to test the proposed system. The signals are sine wave, square wave and triangular wave with an amplitude of 500mVpk-pk at a frequency of 100 Hz. Those signals are generated using GW INSTEK GFG-8020H function generator, and used as the input signal to the audio codec. The input signal and output signal of the audio codec are measured and observed using Tektronix TDS 2022b oscilloscope. The experimental setup is illustrated in Figure 9.8.

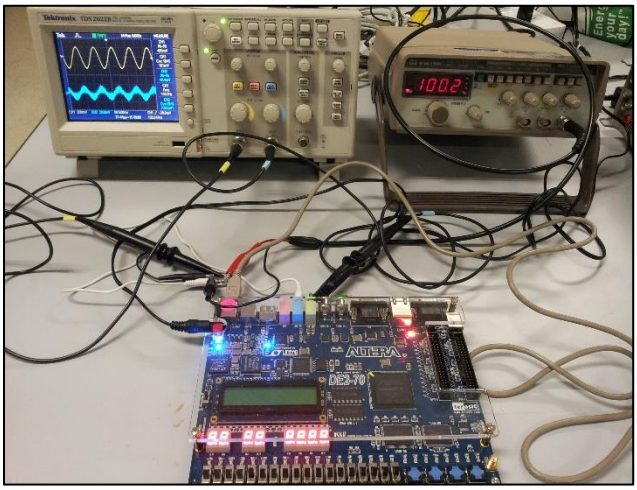

Figure 9.8: Experiment setup

9.4 Results and discussion

The microprocessor system is running in Cyclone II EP2C70F896C7 FGPA chip and is interfaced with the audio codec, the Wolfson WM8731L chip on the Altera DE2-70 board. The audio input of the audio codec is connected to a function generator. Both the input and the output of the audio codec are connected to the oscilloscope. An analysis is carried out to compare the input signal and output signal of the audio codec through the oscilloscope.

Three different input signals are applied to the audio codec separately in order to observe and analyse the output response of each input signal. Figure 9.9, Figure 9.10 and Figure 9.11 show the input signal from the function generator to the audio codec chip (yellow line) and the output signal from the audio codec chip (cyan line). The input signal and the output signal are captured using the auto range feature in the oscilloscope. In Figure 9.9, the input signal is a 100.6 Hz sine wave with 472 mVpk-pk and the output signal is a noisy sine wave with 41.6 mVpk-pk. In Figure 9.10, the input signal is a 100.8 Hz triangle wave with 456 mVpk-pk and the output signal is a noisy triangle wave with 36.0 mVpk-pk. In Figure 9.11, the input signal is a 100.2 Hz square wave with 488 mVpk-pk and the output signal is a noisy square wave signal with 50.4 mVpk-pk. In Figure 9.11, the amplitude of the output signal is decreased at the point after the rising edge to the point before the falling edge. Based on Figure 9.9, Figure 9.10 and Figure 9.11, the output signal is slightly shifted in phase by 2 ms to 3 ms as compared to the input signal. This

may be due to the time taken for the transfer of data between memory and audio codec by the microprocessor.

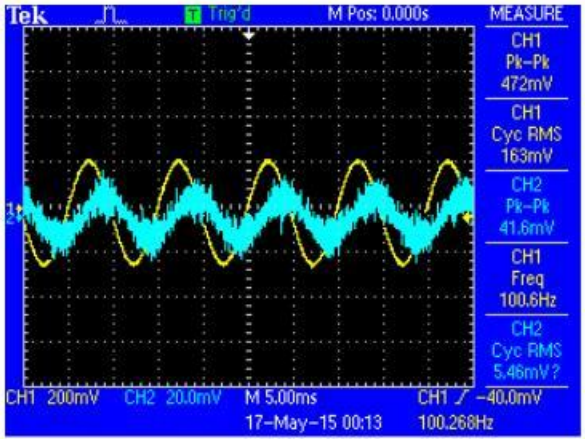

Figure 9.9: Oscilloscope measurement for sine wave input signal

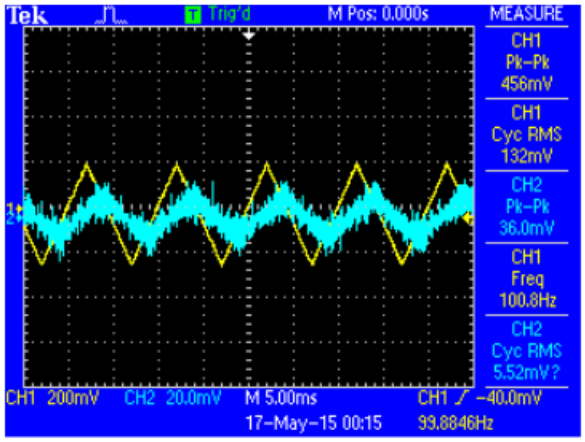

Figure 9.10: Oscilloscope measurement for triangle wave input signal

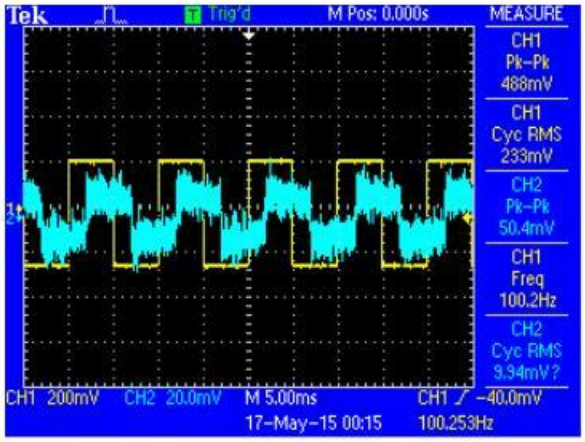

Figure 9.11: Oscilloscope measurement for square wave input signal

According to the PowerPlay Analysis tool in Quartus II, the total reported thermal power dissipation for the architecture is 208.21 mW. The core static power dissipation is 155.00 mW and the I/O thermal power dissipation is 52.46 mW. The measurement output is based on the vectorless estimation toggle rate.

The microprocessor system can function as an audio player or audio recorder. An additional memory component or storage facility are suggested to be inserted in the system to enable a longer recording time or longer playback time. The system can also be used as a signal processing system by implementing a signal processing algorithm. Examples of signal processing algorithms include speech recognition, stethoscope and audio signal processing [3], [4], [6], [8]. In the future, this work will further improve the proposed real-time audio signal processing system and verify it in the FPGA board.

9.5 Conclusion

In this chapter, the implementation of a microprocessor system interface with an audio codec is carried out and the system is observed and analysed. In this work, a microprocessor system is designed, synthesized using Quartus II software and programmed using Nios II SBT. An experiment is carried out to observe and analyse the output signal from the microprocessor system interface audio codec with various input signals. The results show that the output signal becomes a discrete analogue signal of 9 to 12 times smaller amplitude compared to the input signal. Based on the power consumption report, the estimated power for the system architecture is 208.21 mW. The future task of research is to develop a real-time audio signal processing system and implement it in the FPGA board.

References

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