A Study on Real-Time Pulse Sensor Interface with System-on-Chip Architecture

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Abstract—The ability to perform real-time signal analysis on physiological signal is important in today's technology. This allows physician to monitor their patient's health condition and provide the necessary action immediately. To obtain accurate measurement of this signal, proper signal interface between the patient body and the signal analyzer is crucial. In this work, a microprocessor system interfaced with an ADC and a pulse sensor is implemented in FPGA hardware. An experiment is carried out to analyze the performance of the system by executing real-time data acquisition system on various test data. From the experiment results, the system is able to achieve good results as compared to the direct measurement using oscilloscope. Based on the power analysis results, the proposed system has total power dissipation around 200.63 mW to 201.17 mW.

Keywords—microprocessor system; pulse sensor; ADC; FPGA.

I. Introduction

Physiological signals from human a very important nowadays to help physician understand the internal activities and condition of a person. These physiological signals can be measured by placing sensors onto the person and analyzing it for disease detection by using a personal computer (PC) or portable microprocessor system. To ensure accurate signal reading between human and the signal analyzer, proper interfacing between the sensor and the signal analyzer is crucial.

Typically, an analog-to-digital converter (ADC) is required for interfacing a sensor with a digital signal analyzer. An ADC converts the analog signal into the equivalent digital value. In selecting this interface, the specification of the ADC, sensors and the signal analyzer has to be taken into account. This is because, the overall system performance is affected by ADC sampling rate, sensors input voltage range, and the signal analyzer processing speed.

In this paper, a microprocessor system interface with ADC and pulse sensor is proposed. Section II discusses several existing systems interfaced with ADC and pulse signal based sensor for biomedical. Section III presents the methodology of implementing a microprocessor system interface with ADC and pulse sensor using Field Programmable Gate Array (FPGA) and its experimental setup. In section IV, the experimental results of microprocessor system with ADC and pulse sensor are discussed in detail. Finally, section V concludes this paper.

II. Literature Review

A pulse signal such as photoplethysmograph (PPG) can be captured by using Programmable System-on-Chip (PSoC) platform for pulse oximeter application [1]. The Pulse Oximeter is used to measure oxygen saturation in a blood and monitor heart rate by using SpO2 Sensor, a transmission type PPG sensor. The Pulse Oximeter system consists of SpO2 sensor, signal generator, amplifier, filter, ADC, SpO2 and Pulse rate detection module and LCD. Fig. 1 illustrates the block diagram of the proposed Pulse Oximeter system. The amplifier converts the current signal from the sensor to voltage, while the filter limits the signal into certain frequency. The system uses a 13-bit resolution ADC. The SpO2 and pulse rate detection module uses peak finding algorithm and displays the detection result on a LCD.
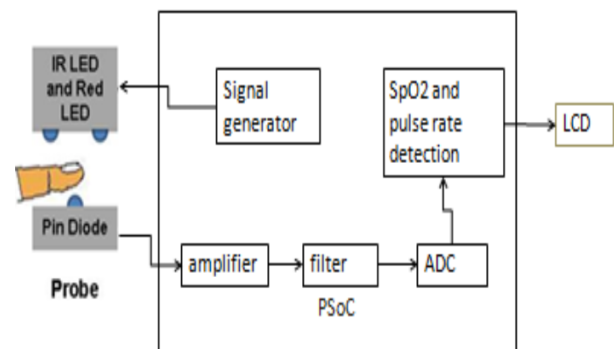

Fig. 1. Block diagram of Pulse Oximeter system [1]

In order to perform a more accurate and efficient measurement, a system requires an analog front-end (AFE) component such as ADC, signal conditioning circuit and a signal processing component. This criteria can be fulfilled by using a configurable and low-power mixed signal System-on-Chip (SoC) as introduced in paper [2]. The SoC is developed for portable ECG monitoring application. The system has a low voltage and high performance AFE, which is able to support 3 channels of ECG signals. It uses a 12-bit successive approximate register (SAR) ADC with adaptive sampling scheme. The system also contains a custom digital signal processor (DSP) for signal analysis algorithm and digital filtering such as R Peak detection and motion artifact removal. SIMD (Single Instruction Multiple Data) processor architecture is used in the custom DSP. Fig. 2 and Fig. 3 illustrate the block

diagram of the analog Front End and the block diagram of custom DSP, respectively. The proposed SoC is reported to have a power consumption of 31.1μW from a 1.2V power supply.
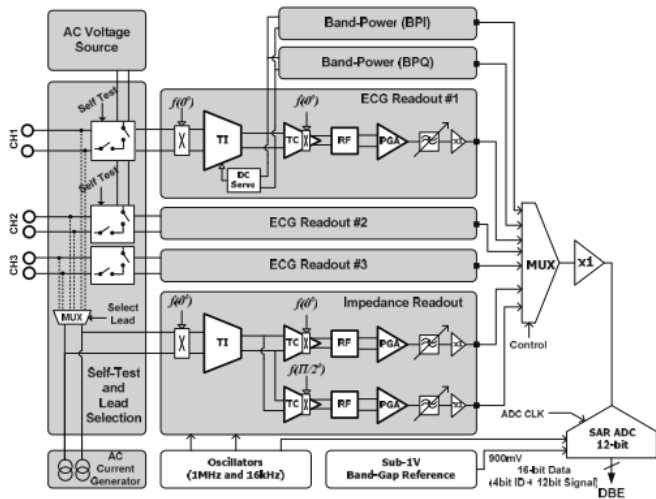

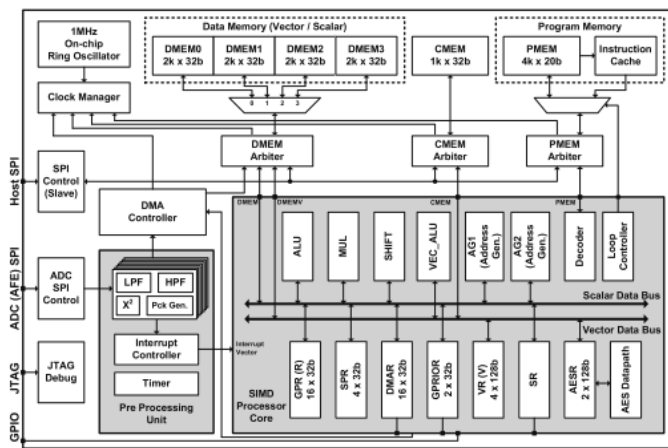Fig. 2.   Block Diagram of the Analog Front-End [2]

Fig. 3.   Block Diagram of Custom Digital Signal Processor [2]

A wireless biomedical monitoring system for a real time ECG signal analysis is presented by authors in paper [3]. The system uses a universal asynchronous receiver/transmitter (UART) based Bluetooth module to transmit data between its master terminal and slave terminal. Both master and slave systems are developed using ARM based SoC platform. In the slave terminal system, the ECG signal data from AFE is measured and converted into digital signal using ADC. A real-time analysis is performed by the signal processor to detect heart rate and heart rate variability. The data is then compressed and sent to the master terminal through Bluetooth wireless communication. At the master terminal, the data that are sent from slave terminal are monitored.

A real-time ECG signal heart rate estimator using a microcontroller based system is presented by the authors in paper [4]. The microcontroller system consists of Atmel 89C51

microcontroller, DAC0808, ADC, LCD display, and I/V converter. Fig. 4 illustrates the block diagram of the microcontroller system. In this paper, a synthetic ECG signal is generated by a personal computer. The DAC and I/V converter then converts the synthetic ECG signal into electrical ECG signal before delivering it to the microcontroller system for real-time heart rate estimation. Once the microcontroller has received the synthetic ECG signal, real-time heart rate estimation is applied to the signal and the result will be displayed on LCD.
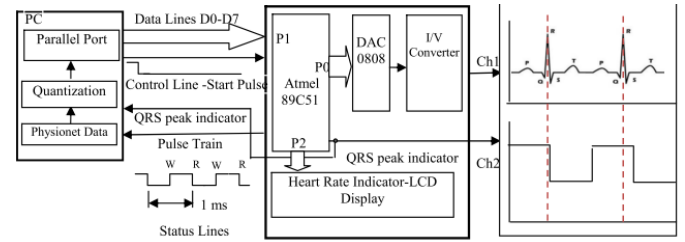

Fig. 4.   Block diagram of the microcontroller system [4]

In paper [5], an effective three way PPG acquiring and signal processing system by using square wave modulation is proposed. The proposed system detects heart rate, oxygen saturation, and pulse wave velocity. Fig. 5 illustrates the overall system architecture of the proposed system. The signal processing system consists of an AFE with light-based PPG sensor, LED driving circuit, anti-aliasing filter, FPGA-based artery pulse information extractor (APIE), and a TI MSP430 microcontroller with built-in ADC. The FPGA-based APIE is used to drive the LED circuit with different wavelengths and to extract the correct signal by the ADC from microcontroller. The anti-aliasing filter eliminates the harmonic signal which may cause aliasing after the sampling process. The system uses a graphic user interface (GUI) to observe PPG signal. It interfaces with the system through serial communication between PC and the microcontroller.
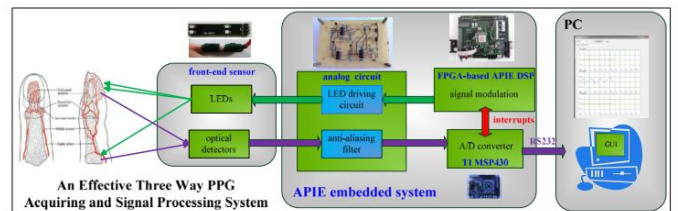

Fig. 5.   Overall system architecture of the proposed three way PPG acquiring and signal processing system [5]

Based on the previous discussion, the important characteristics of the existing system are tabulated in Table I. Among these systems, a majority of the systems uses a microprocessor as part of the signal processing component for algorithm and also controls the overall system. Various microprocessor types are used in these systems depending on user preference such as DSP, ARM processor, 8051 processor and MSP (mixed signal processor). In addition, some of the systems used a system with built-in ADC, which allows direct data transfer within the system. However, for higher sampling resolution, a discrete ADC chip is preferred as implemented in

paper [1], [2]. Based on Table I, a majority of the reported pulse based signal related application for biomedical analyzed either ECG or PPG application. In this application, peak detection and interval detection algorithm is widely used to analyze the signal.

TABLE I. COMPARISON OF EXISTING MICROPROCESSOR SYSTEM WITH ADC FOR BIOMEDICAL APPLICATION

	[1]	[2]	[3]	[4]	[5]
Processor	Not stated	Custom DSP	ARM	Atmel 89C51 μc	TI MSP430
ADC	13-bit ADC	12-bit SAR ADC	Yes	Yes	μc Built-in
Application	Heart rate and oxygen saturation in blood using PPG signal	ECG Monitoring	Wireless ECG monitoring	Real time heart rate estimation from ECG signal	PPG signal analysis
Algorithm	SpO2 and pulse detection	R peak	R peak and HRV analysis	QRS detection	heart rate detection, oxygen saturation, and pulse wave velocity
Hardware	PSoc	SoC	FPGA	ASIC	ASIC & FPGA

III. METHODOLOGY

In this section, our proposed microprocessor system interfaced with ADC and pulse sensor is explained in detail. The proposed microprocessor system consists of a Nios II economy version processor, 32 MB SDRAM with its memory controller, 64 kB on-chip memory, timer module, Avalon bus, Joint Test Action Group (JTAG) universal asynchronous receiver transmitter (UART) and GPIO. An 8-bit microprocessor compatible ADC from National Semiconductor, ADC0804, is used for signal conversion between pulse sensor and microprocessor system. ADC0804 is an 8-bit successive approximation ADC and has one differential analog voltage input. The analog input of the ADC0804 is connected to the pulse sensor output and the 8-bit digital output of ADC0804 is connected to the GPIO of the microprocessor system. The block diagram of the microprocessor system with ADC and pulse sensor is illustrated in Fig. 6.

The pulse sensor used in this work is an optical-based heart rate sensor with model name of SN-PULSE from Cytron Technologies [6]. The pulse sensor is easy to interface with microprocessor system where it operates using 5V power supply. In addition, the sensor has only a single analog output and it has built-in amplification and noise cancelation circuit that improves the output signal. It's analog signal output has a voltage range of 0V to 5V. The output signal level depends on the reflected or absorbed light by the skin tissue when the device is applied to human finger.
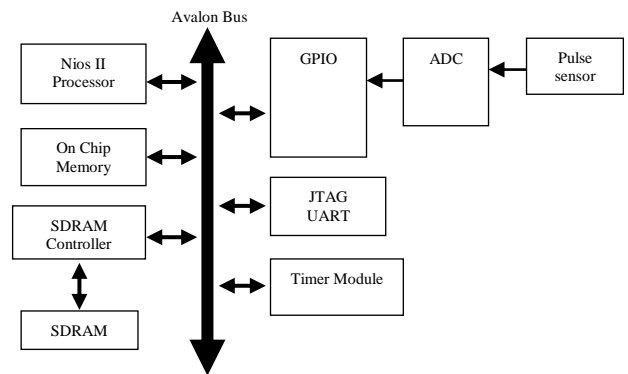

Fig. 6. Block diagram of Microprocessor system with ADC and Pulse sensor

In order to interface with the pulse sensor, ADC0804 has been selected as a data converter between the microprocessor system and pulse sensor. It interfaces with microprocessor using 8-bit parallel data port. ADC0804 has analog input signal level that matched with the output range of the pulse sensor. Once the analog input signal is received, the signal level is converted into 8-bit binary data by the ADC using successive approximate register method [7]. The 8-bit digital output from the ADC0804 is connected to a GPIO where 8-bit binary data is sent to the microprocessor system. In this research, free-running mode circuit configuration for ADC0804 is selected where the analog input is converted into digital output automatically by the internal clock. An RC circuit that consists of 150pF capacitor and 10k ohm resistor is used as a clocking circuit for ADC0804, which allows the ADC to self-clock instead of using an external clock. With the configuration, a conversion time of approximate 100μs is required for analog input to be converted into digital data completely. The configuration of ADC0804 used for this work is illustrated in Fig. 7.
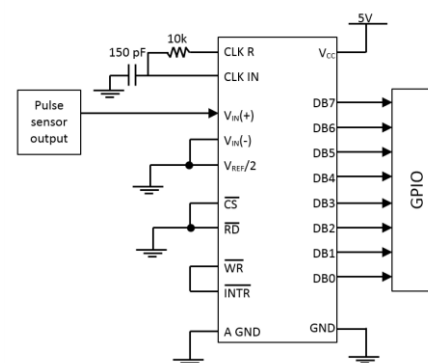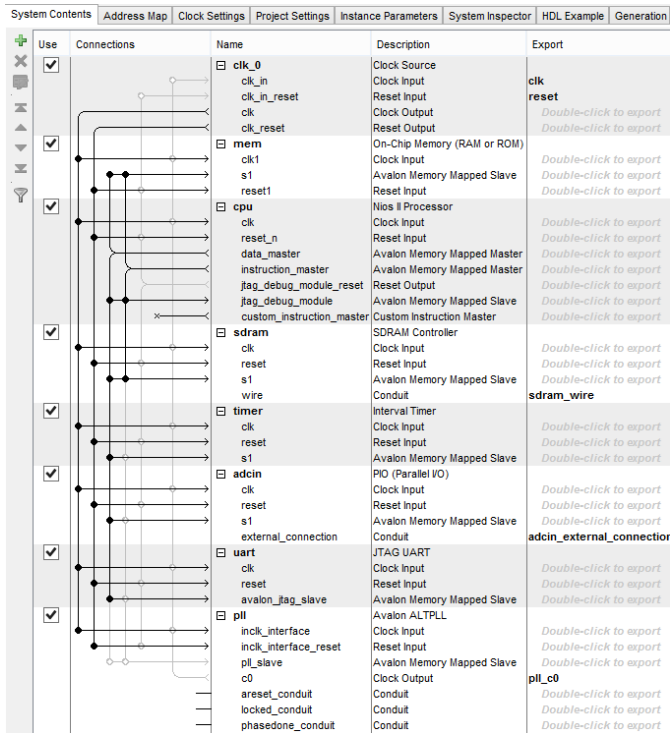

Fig. 7. Configuration of ADC0804

The microprocessor system is developed and synthesized using Quartus II software. Qsys tool from Quartus II software is used to integrate system component and processor into a microprocessor system. The microprocessor system is synthesized and the I/O of the system is assigned by Quartus II software. Quartus II programmer is used to download the synthesized hardware design along with I/O assignment into Cyclone II EP2C70F896C7 FGPA chip in Altera DE2-70

Board. Fig. 9 shows the system interconnection of the proposed system in Qsys tool based on the block diagram illustrated in Fig 7. In Fig. 8, a phase-locked loop (PLL) module is used to provide 50 MHz -0.3 ns shifted clocked pulse to SDRAM.

Fig. 8.   System interconnection of the proposed microprocessor system in Qsys

To program the processor, the microprocessor system is programmed by Nios II Software Build Tool. Nios II Software Build Tool is a tool chain for Nios II processor where it is used to compile application program for the processor as well as providing driver and hardware abstraction layer (HAL) support to the processor. Nios II Software Build Tool is also used to download the application program into the program memory for the microprocessor system.

In this work, an application program is developed to perform data acquisition. In the program, a timer module is used as a timer interrupt to capture the data from the ADC digital output through GPIO in a fixed interval period. This is to allow the microprocessor system to capture the data periodically. To test the system performance, an experiment is performed onto the system. In the experiment, three different timer interval periods are set on the timer modules. The interval periods are 1ms, 500µs, and 100µs, which represent the equivalent sampling rate of 1kS/s, 2kS/s and 10kS/s, respectively (kS/s denotes kilo sample per second).

In data acquisition program, a total of 20,000 data from the ADC output is collected to observe, analyze and evaluate the performance of ADC and the output of the pulse sensor. Three experiments are designed with this program to collect the data from the ADC. The first two experiments use sinusoidal frequency input signal generated by using GW INSTEK GFG-8020H function generator. The frequencies of sinusoidal input

signal used in the experiment are 1Hz and 10Hz. The third experiment uses human pulse signal taken from finger by using the pulse sensor.

IV. RESULTS AND DISCUSSION

In the previous section, we have discussed the experimental setup for our work. In this section, we will discuss the result obtained from our experiments. The purpose of the first two experiments is to test and validate the functionality of the ADC interfaced by microprocessor system. The purpose of the third experiment is to test the capability of microprocessor system interfaced with ADC in capturing real-time pulse signal from human.

Each data is retrieved from the ADC and stored in SDRAM when timer interrrupt is called. A total of 20,000 data is stored in the SDRAM. The data from the experiment is tabulated and plotted into graphs by using Matlab software. Three different signals are used for testing in the proposed system. These signals are 1Hz and 10Hz frequency of sinosoidal signal with amplitude range of 0V to 5V and a human pulse signal from a pulse sensor that is attached on human finger. The proposed system is illustrated in Fig. 9.
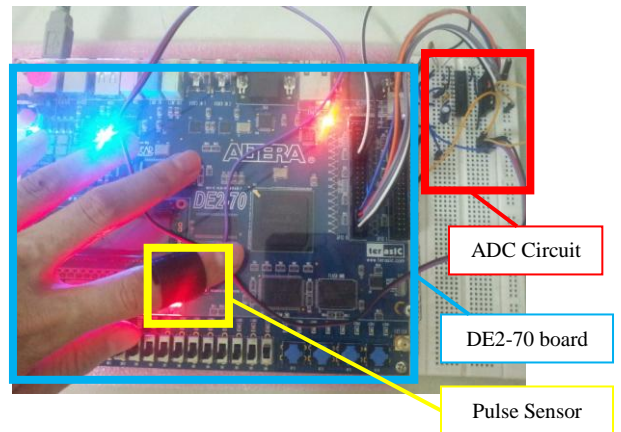

Fig. 9.   DE2-70 FPGA board with ADC0804 circuit and pulse sensor with human finger attached

The proposed system is tested with three different periods of timer where each represents the sampling rate of the data. Three different graphs are produced for each of the tested signal. Fig. 10 presents the 1Hz frequency of sinosoidal signal with total time of 1s. The purpose of using 1Hz frequency of sinosoidal signal is to mimic the condition of a human pulse signal or heart rate, which is approximately 1 Hz to 2 Hz [8]. Based on Fig. 10, the sampling rate of 1kS/s to 10kS/s is capable of measuring input signal with 1Hz of frequency.

As the input signal frequency increased to 10 Hz, the graph illustrated in Fig. 11 shows that the proposed system is able to capture 10Hz frequency sinusoidal signal. In Fig. 11, 10 Hz frequency of sinusoidal signal is presented in a period of 1s. With the free-running mode configuration of the ADC based on the datasheet in [7], the ADC has a conversion time of approximately 100µs, which is equivalent to a 10 kHz conversion rate. Thus, the proposed system is capable to sample data up to 10 kHz with the selected ADC.
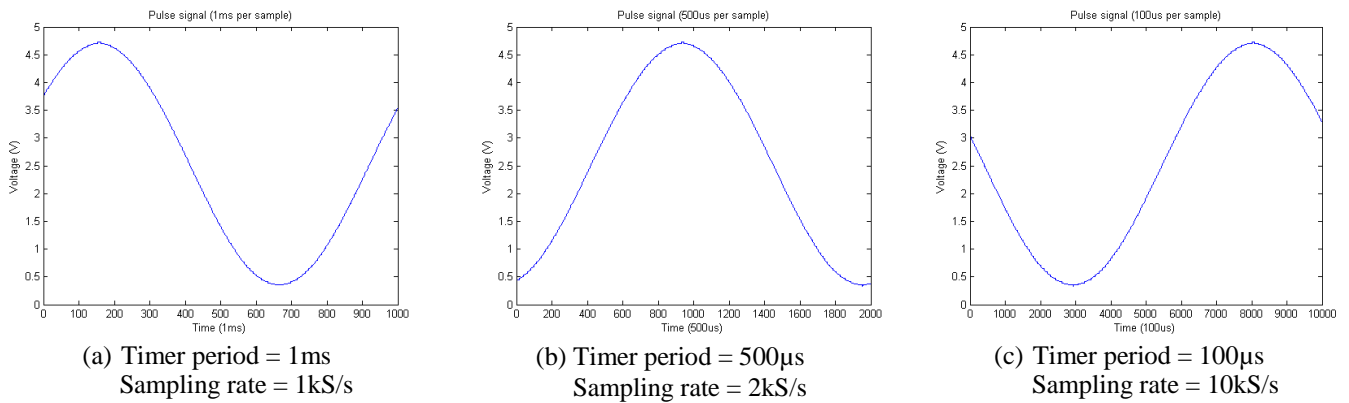
(a) Timer period = 1ms
Sampling rate = 1kS/s

(b) Timer period = 500µs
Sampling rate = 2kS/s
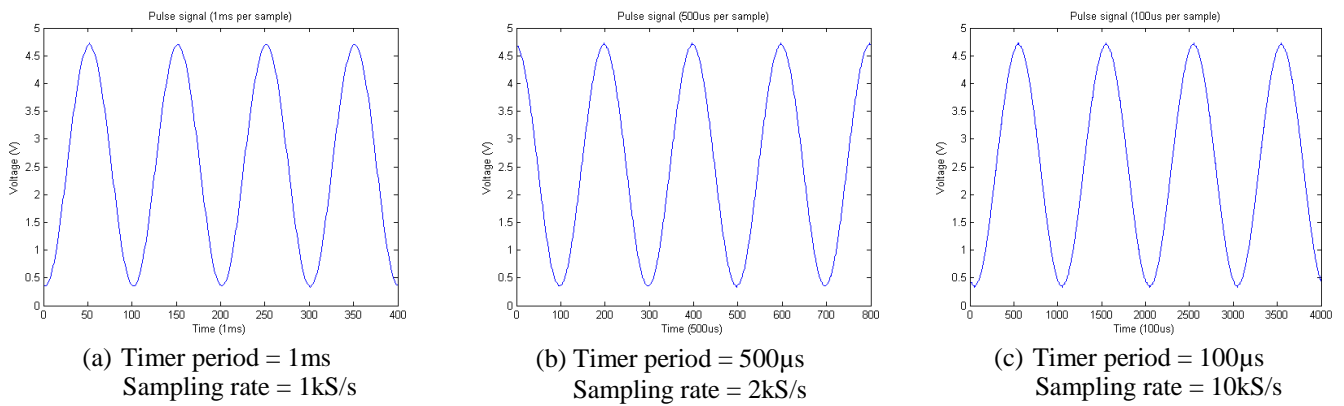
(c) Timer period = 100µs
Sampling rate = 10kS/s

Fig. 10. 1Hz sinosoidal signal is measured by the proposed system with sampling rate of 1kS/s, 2kS/s and 10kS/s

(a) Timer period = 1ms
Sampling rate = 1kS/s

(b) Timer period = 500µs
Sampling rate = 2kS/s

(c) Timer period = 100µs
Sampling rate = 10kS/s

Fig. 11. 10Hz sinosiodal signal is measured by the proposed system with sampling rate of 1kS/s, 2kS/s and 10kS/s

(a) Osciloscope

(b) Timer period = 1ms
Sampling rate = 1kS/s

(c) Timer period = 500µs
Sampling rate = 2kS/s
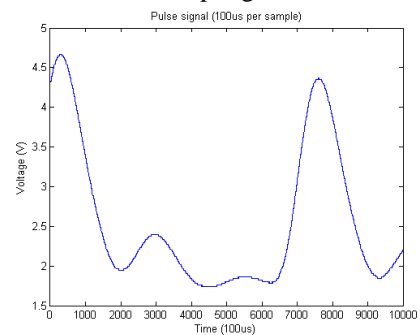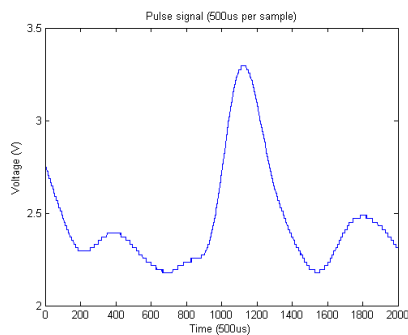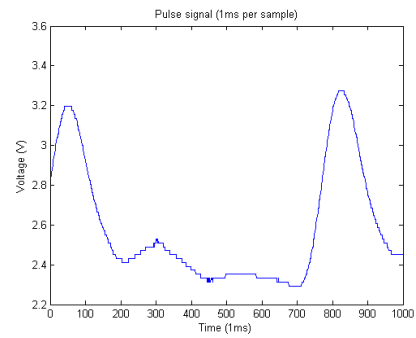
(d) Timer period = 100µs
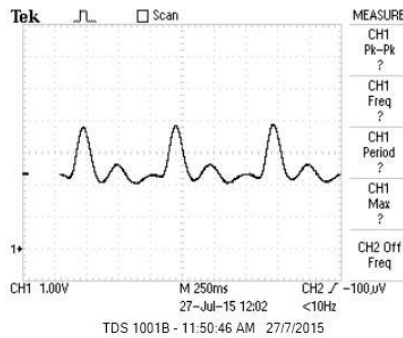Sampling rate = 10kS/s

Fig. 12. Raw signal measured from pulse sensor attached on human finger by oscilloscope and proposed system with sampling rate of 1kS/s, 2kS/s and 10kS/s

Next, a pulse signal is measured from pulse sensor that is attached to human finger. Fig. 12 illustrates the human pulse signal measured directly by an oscilloscope and by our proposed system with different timer configuration in a period of 1s. The pulse signal shown in Fig. 12 (a) is observed directly from the signal recorded by Tektronix TDS 2022b Oscilloscope. By comparing the measured pulse signals using pulse sensor with different timer configurations in microprocessor system, the quality of the pulse signal recorded with higher sampling rate can be studied.

From Figure 12 (b) to (d), the output from the system matches closely with the output from the oscilloscope. This proves that the system is able to perform similar reading as compared to the oscilloscope output. Furthermore, this validates that the data flow between the system modules such as microprocessors, SDRAM and GPIO work correctly.

By observing the signal in Fig. 12 (b), the measured signal at sampling rate of 1kS/s shows an obvious constant 'staircase' shape. Moreover, a certain part of the signal is flickered (example at time of 450). In Fig. 12 (c), the signal with sampling rate of 2kS/s has similar 'staircase' shape but with less flickering effect compared to the signal in Fig. 12 (b). The signal with sampling rate 10kS/s as shown in Fig. 12 (d) has a better shape than the signal in Fig. 12 (b) and Fig. 12 (c). This is because the sampling rate for signal in Fig. 12 (d) is 10 times higher than sampling rate for signal in Fig. 12 (b) and 5 times higher for signal in Fig. 12 (c).

Table II summarizes the Quartus II compilation report for the proposed system with different timer settings. From the table, the average total logic element for the proposed system is 2503.33. The PowerPlay Power Analysis is carried out using 12.5% of default toggle rate for input I/O signal and the toggle rate of remaining signals is vectorless estimated. From the PowerPlay Power Analyzer report, the average total thermal power dissipation for the proposed system is 200.89 mW where the average core static thermal power dissipation is 154.97 mW and the average I/O thermal power dissipation is 44.92 mW.

TABLE II.   TOTAL LOGIC ELEMENTS AND POWER DISSIPATION FOR THE PROPOSED EMBEDDED SYSTEM

Interval period of Timer Modules	Total Logic Elements	Total Thermal Power Dissipation	Core Static Thermal Power Dissipation	I/O Thermal Power Dissipation
1ms	2,520	200.87 mW	154.97 mW	44.92 mW
500µs	2,496	200.63 mW	154.97 mW	44.92 mW
100µs	2,494	201.17 mW	154.98 mW	44.92 mW
Average	2503.33	200.89 mW	154.97 mW	44.92 mW

V. CONCLUSION

In this paper, a microprocessor system interfaced with ADC and pulse sensor is implemented in FPGA. Several existing microprocessor systems with pulse signal based sensor are reviewed. An experiment is carried out to analyze the functionality and performance of the proposed microprocessor system interfaced with ADC. In the experiment, an application program is downloaded to the microprocessor system to perform as a data acquisition system where 20,000 input data is stored for analysis. Based on the result, the system output is able to match closely with the output taken directly from the oscilloscope. Furthermore, higher sampling rate produces a better resolution in measurement especially for pulse sensor output signal. Based on the power analysis results, the proposed microprocessor system has an average power dissipation of 200.89 mW. In future work, a peak detection algorithm will be implemented into the microprocessor system together with ADC and pulse sensor to perform automatic heart rate detection.

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