Automatic Peak Detection System Power Analysis Using System on a Programmable Chip (SoPC) Methodology

Lim Chun Keat[1], Asral Bahari Jambek[2] and Uda Hashim[3]
[1,2]School of Microelectronic Engineering, Universiti Malaysia Perlis, Perlis, Malaysia
[3]Insituite of Nano Electronic Engineering, Universiti Malaysia Perlis, Perlis, Malaysia
Email: [1]wally.ck24@gmail.com, [2]asral@unimap.edu.my, [3]uda@unimap.edu.my

***Abstract*—In this paper, a power analysis of a Nios II processor system is carried out. The methodology of power analysis includes SoPC (System on a Programmable Chip) system integration, architecture design compilation, software program compilation using a toolchain, system simulation and power analysis. In this work, a peak detection algorithm is implemented into the embedded processor system for power analysis. Several toggle rate settings are applied to the power analysis on the system architecture using the PowerPlay Power Analyser. Based on the power dissipation report, the estimated total power consumption is between 198.86 mW to 258.15 mW, while the core static power consumption is from 154.97 mW to 155.17 mW. The results show that performing power analysis with a higher number of signal activities means it is possible to increase the accuracy of the estimated power consumption.**

Keywords— Power analysis; FPGA; NIOS II; PowerPlay Power Analyser.

I. INTRODUCTION

System on a Programmable Chip (SoPC) is an alternative method to System on Chip (SoC). It applies a field programmable gated array (FPGA) design approach by integrating intellectual property (IP), such as the processor core and custom module, into a SoC. Compared with a traditional SoC, it is flexible in design and takes less time to produce [1]. However, the power consumption of FPGA may not be lower than an application specific integrated circuit (ASIC) SoC [2]. This is because the power consumption of the system depends on the complexity of the system or application [1].

There are a number of factors that can affect the power consumption in an integrated circuit (IC), such as current leakage and heat dissipation, which can affect the performance of the integrated circuit [3]. In an FPGA chip, power management is important. The power consumption is separated into two components: static power consumption and dynamic power consumption [4],[5]. Static power is the power consumed by itself without any operation by a transistor, while dynamic power is the power consumed by the switching activities of transistor inside the chip that causes the charging and discharging of load capacitance [6]. Furthermore, the power consumption for the input and output terminals needs to be considered. This is due to the general purpose input/output architecture of the FPGA chip [7]. However, dynamic power consumption is the major concern in FPGA.

In this paper, a power analysis methodology of an SoPC is carried out. Section II discusses several power analysis methodologies on an architecture, while section III presents an approach to power analysis on the embedded processor system. In section IV, the power analysis result with different configurations is discussed. Finally, section V concludes the paper.

II. LITERATURE REVIEW

In paper [8], a power estimation method is proposed to estimate the dynamic power consumption of a processor-based design. A MicroBlaze-based processing unit as illustrated in Fig. 1 consists of a single MicroBlaze processor, a timer, an interrupt controller IPs and an AXI bus is used for case study. This hardware design was implemented into a Virtex-6 FPGA ML605 Evaluation kit using Xilinx ISE Design Suite 14.4. Two versions of five different hardware designs with three different C program applications are selected for power estimation. The power consumption of the hardware design is measured by using the Xilinx Chip scope tool and is estimated by the XPower Analyser tool. Based on the result, the dynamic power consumption of the hardware design is estimated to be 84 mW to 102 mW.

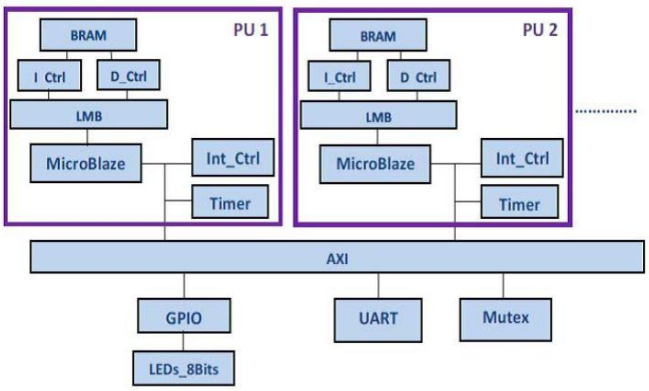

Fig. 1. Hardware design for power estimation [8]

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The author in paper [9] presents a very low power and high throughput Advanced Encryption Standard (AES) processor. The encryption process of AES for the proposed processor is illustrated in Fig. 2. The proposed processor is simulated on Stratix II GX family FPGA using Quartus II software. In order to study the power consumption, the PowerPlay Early Power Estimation Tool is used to approximate the power consumption and the PowerPlay Power Analyser is used to estimate the static and dynamic power consumption of the proposed processor. The PowerPlay Analyser tool analyses the power consumption of the architecture with the Quartus II CSV file and the static and dynamic power estimation is carried out by using the PowerPlay Power Analyser using the VCD and SAF file of the simulated output. The power analysis flow for Quartus II using the PowerPlay Early Power Estimation Tool and the PowerPlay Power Analyser is illustrated in Fig. 3. In [9], two different clock frequencies are used to examine the dynamic power consumption of the proposed design.

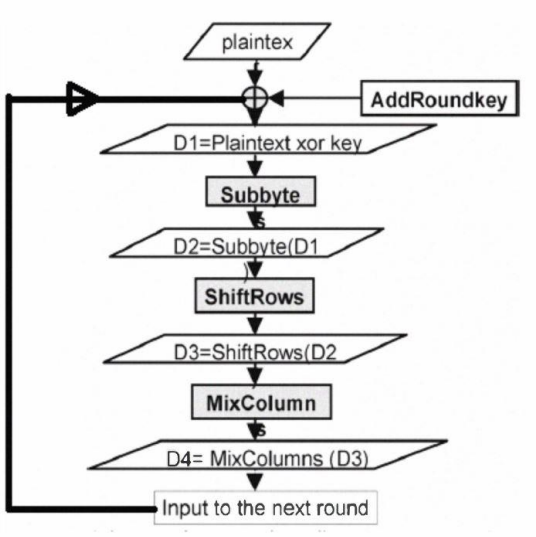

Fig. 2. Encryption Process of AES [9]

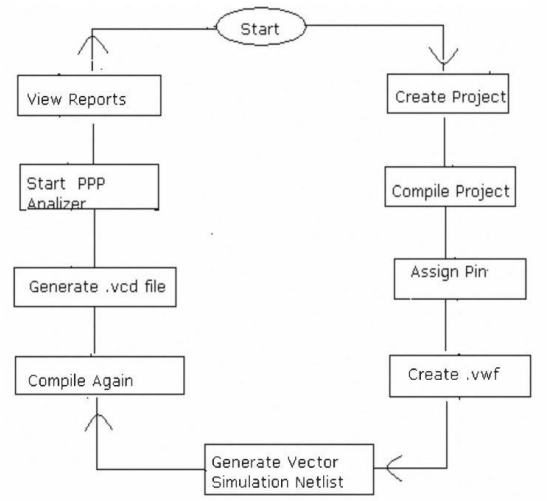

Fig. 3. Quartus II Power Play Power Analyser Schematic [9]

VersaPower, a power estimation tool for FPGA architecture, is presented in paper [10]. The power estimation tool or power model is designed to work with the Versatile Place and Route architecture (VPR) design tool. The design flow of the VPR tool is illustrated in Fig. 4. In the design flow, ODIN II is used for design synthesis, ABC (a logic synthesis and verification tool) is used for optimization and VPR 6.0 is used for placement and routing. In power estimation, the activities signal, the design architecture in FPGA and a power model is used to estimate the dynamic and static power of the architecture. Altera Stratix IV FPGA architecture is used for power analysis. In the architecture analysis, several designs are tested to obtain the power consumption.

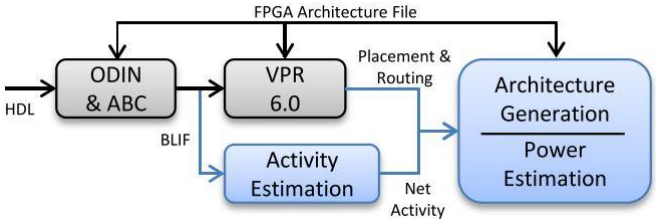

Fig. 4. VPR design flow for power estimation [10]

The authors in paper [11] present a power analysis of Joint Photographic Experts Group (JPEG) encoder architecture in FPGA. The JPEG encoder architecture. The architecture contains three main components: foundation compression, Discrete Cosine Transformation (DCT) and additional compression. The architecture was implemented in Xilinx Spartan-3E and its power dissipation is estimated using the Xilinx Xpower tool. The power consumption of the architecture was evaluated using clock frequency from 0.5 Mhz to 1,000 Mhz. Based on the results, the architecture with higher frequency consumed more power than that with lower frequency. Another experiment also proved that using a glitching technique can decrease the power dissipation of the architecture.

A solution for leakage power reduction in FPGA DSP circuits is introduced by the authors in paper [12]. This power reduction method is implemented by applying a new Algorithmic Noise Tolerance (ANT) method. An FIR filter with and without ANT is selected as the test target for power analysis. The target is tested in architecture as shown in Fig. 5, where an 8-bit grayscale image was applied to the target. The power analysis is carried out by measuring voltage drop across the resistor using a high-precision digital multi-meter (DMM) and estimated using the PowerPlay Power Analyser. Based on the result, a filter that incorporates ANT achieves 15% less static power than a filter without ANT.

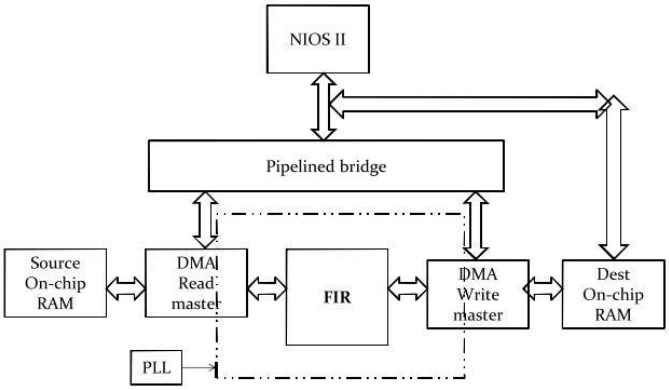

Fig. 5. Block diagram of the test system [12]

Several existing power analysis methods for various types of architecture in FPGA are reviewed. The existing power analysis methodologies are detailed in Table I. Based on Table I, the architectures that undergo power analysis are either processor-based architecture or application-specific architecture. The architecture is implemented in either a Xilinx or Altera FPGA, such as Xilinx Virtex-6, Altera Stratix II GX, Xilinx Spartan-3E and Altera Stratix IV. For Xilinx FPGA, the power analysis is carried out by using the Xilinx ChipScope tool and the Xilinx XPower tool, while the power analysis for the Altera FPGA is carried out using the PowerPlay Early Power Estimator and the PowerPlay Power Analyser. An open source design tool, the VPR tool is used for architecture design, whereas the VersaPower tool is used in conjunction with the VPR tool for power estimation on the architecture. Besides,Power consumption also can be measured using DMM on the FPGA board.

TABLE I. COMPARISON OF EXISTING POWER ANALYSIS METHODOLOGIES IN FPGA

	[8]	[9]	[10]	[11]	[12]
Architecture	MicroBlaze based processing unit	AES processor	Logic Circuit	JPEG Encoder	Nios II processor system
FPGA	Xilinx Virtex-6	Altera Stratix II GX	Altera Stratix IV	Xilinx Spartan-3E	Altera Stratix IV
Power Analysis tool	Xilinx ChipScope tool & Xilinx XPower tool	PowerPlay Early Power Estimation & PowerPlay Power Analyser	Versa Power	Xilinx XPower tool	DMM measurement & PowerPlay Power Analzyer
Application	Power estimation	AES	Power estimation	Image compression	Leakage Power reduction

III. METHODOLOGY

In this section, a methodology of power analysis on the embedded processor system will be explained. The methodology involves several steps, including system on a programmable chip (SoPC) design, design compilation, application program compilation, simulation and power analysis. The flow chart in Fig. 6 presents the methodology of the power analysis. In this work, the embedded processor system as illustrated in Fig. 7 contains a Nios II processor, on-chip memory, Synchronous Dynamic Random Access Memory (SDRAM) with its controller, general purpose input/output (GPIO) port, JTAG UART and Avalon Bus. For the proposed system, the Nios II economy version processor is used.

The proposed system is developed using an SoPC design approach. This approach integrates all the components with an interconnection in a system and implements them on the FPGA chip. Through this approach, the system architecture is designed and synthesized using a system integration tool, the Qsys tool from Quartus II software [13]. In the Qsys tool, system components such as a Nios II processor core, memory controller and on-chip memory module, among others, are interconnected together with the Avalon Bus. Once the system architecture is generated, the architecture with I/O contact is synthesized, fitted and assembled by Quartus II software, based on the target FPGA model. In this work, Cyclone II EP2C70F896C6 was selected as a target for design compilation.

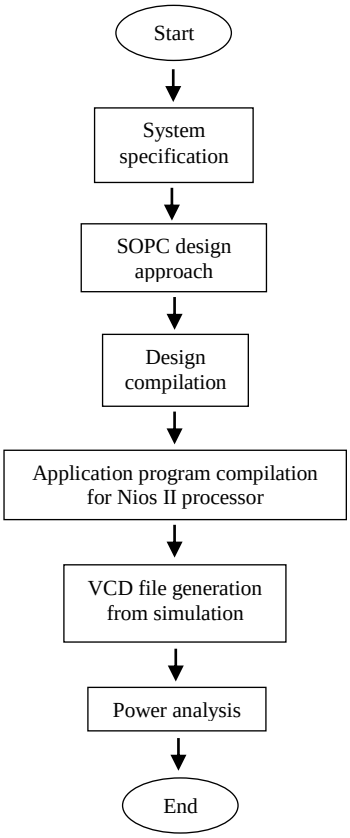

Fig. 6. Methodology of power analysis on Nios II processor-based system

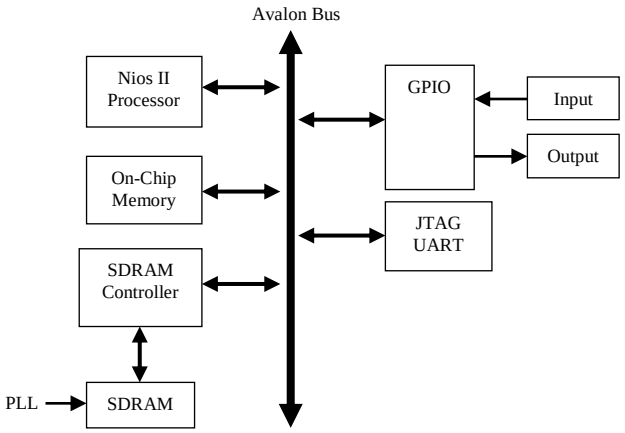

Fig. 7. Block diagram of the proposed peak detection system

In order to analyse the power consumption of a running system, a peak detection algorithm is implemented on the embedded processor system. The peak detection algorithm mimics the "findpeaks" function in the Matlab software [14]. This algorithm performs peak finding on a signal and stores the number of peaks, peak amplitude and gap between peaks. 1000 of data point is generated randomly by the Matlab software and are used as a target signal. These data are stored in an on-chip memory for the system to read. The algorithm is written in C programming code. This source code is compiled and a hex file generated using the Nios II processor tool chain, Nios II software building tools (SBT) for Eclipse.

Once the hex file is generated, the system architecture with the application program is simulated in ModelSim software [15]. The purpose of performing simulation on the system architecture with the application program is to collect the signal activities within the system architecture. This can be done by generating a value change dump (VCD) file during simulation. The VCD file contains header information, variable definition and variable value changes where the variables are the signals. In order to capture signal activities for a completed cycle of peak detection algorithm on the system, 10ms of signal activities are recorded. These signal activities are used in power analysis to obtain a more accurate result. In applying the VCD file for power analysis, the signal name of the architecture and the variable name in the VCD file must match. Otherwise, the signal activities will not be accounted for in the power analysis.

Next, the power consumption of the system architecture is estimated using the PowerPlay Analyser tool in Quartus II software [16]. In this work, the PowerPlay power optimization is set to normal compilation. In order to analyse the power consumption of the system architecture, the power analysis is run with five different power analyser configurations, such as default toggle rate use vectorless estimation, default toggle rate use 12.5%, toggle rate based on static probabilities generated from the VCD file and a combination of these toggle rate configurations. The static and dynamic power dissipation with various configurations are analysed. A detailed thermal power dissipation is discussed by the architecture hierarchy in Section IV.

IV. Results and Discussion

The embedded processor system architecture is developed as explained in the methodology. A power analysis is carried out on the system architecture based on the Cyclone II EP2C70F896C6 FPGA chip. Various configurations on the PowerPlay Power Analyser are run for analysis. The report power consumption is displayed by Quartus II software, as illustrated in Fig. 8. The power analysis report shows four types of power dissipation: total thermal power dissipation, core dynamic thermal power dissipation, core static thermal power dissipation and I/O thermal power dissipation. These power dissipations are different when a different toggle rate is applied. Hence, various types of power dissipation are tabulated in Table II according to the Power Analyser configuration.

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Mon Oct 19 11:34:12 2015
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	peakdet
Top-level Entity Name	peakdet
Family	Cyclone II
Device	EP2C70F896C6
Power Models	Final
Total Thermal Power Dissipation	200.44 mW
Core Dynamic Thermal Power Dissipation	1.28 mW
Core Static Thermal Power Dissipation	154.97 mW
I/O Thermal Power Dissipation	44.19 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig. 8. Power consumption report for system architecture produced by PowerPlay Power Analyser with vectorless estimation toggle rate

Based on Table II, power analysis that runs using I/O signal activities data and vectorless estimation toggle rate for the rest of the signal consumes more power compared with other configurations. This is because the I/O signals toggle rate estimated based on signal activities obtained from the VCD file. Furthermore, the toggle rate for the remaining signals is estimated based on I/O signal activities and logic function at the nodes in the architecture. In this configuration, it has high core dynamic power, which indicates high activity rate on the architecture or in the internal structure of the FPGA. Power analysis that applies vectorless estimation toggle rate on all signals achieves less power consumption than using I/O signal activities data. This is due to the fact that the signal toggle rates are based on the logic function at the node of the signals in the architecture, which is less accurate.

A more accurate power analysis result is the power analysis that uses available signals obtained from the VCD file while the unavailable signals are vectorless estimated. In this case, around 17% of signals use toggle rate based on the VCD file and the other signal activities are either not recorded in the VCD file or have a different signal name. One of the difficulties in carrying out the power analysis is being unable to match the signal name from the VCD file generated from simulation and from the system architecture compiled by Quartus II. This issue is due to implementing the Nios II processor into a system in which some of the signal names are unknown and being unable to adjust the signal name for power analysis through Quartus II software. In this configuration, 35.06 mW of Core dynamic power dissipation is estimated,

which is slightly lower than the highest core dynamic dissipation.

The input and output power dissipation is nearly identical for any signal toggle rate setting. The core static power dissipation also uses nearly the same power consumption. This is because the system architecture used for power analysis is the same. By using a default toggle rate of 12.5% for all signals, the total power consumption is reported to be the lowest compared with other power analyser configurations. This is because it uses a lower toggle rate but fewer signal activities. This power analysis is considered less effective. The same is true for power analysis with I/O signal activities where the remaining signals use a 12.5% toggle rate.

As a further investigation, the power analysis is examined through hierarchy architecture and by block type. Power analysis that runs with I/O signal activities with the remaining signal using vectorless estimation toggle rate is selected for this analysis. The power consumption report by block type is illustrated in Fig. 9. This allows a better view of power consumption in an FPGA in which the power consumption is categorized by block. In Fig. 9, it can be seen that the M4K block, a memory component block, has a high total power dissipation, while the I/O block has the second highest power consumption. This is due to the application program that performs read and write on on-chip memory and also retrieves program instruction to run the system. It can also be seen that, in addition, it has high block thermal dynamic power. While other block types consume less power.

In power analysis by hierarchy, the on-chip memory component in the system architecture consumed the most power, at 32.02 mW. The CPU or processor component of the architecture, as the second highest power consumer, only took 5.63 mW power, while the JTAG UART component only consumed 1.26 mW of power. The rest of the components in the system architecture took less than 1 mW of power.

In order to achieve a better accuracy of power analysis on FPGA, a VCD file generated from simulation for all signals is required. The simulation period must be a full cycle of the application program. All the signal names in the VCD file and in the power analysis tool must be matching. Lastly, the power analysis results for FPGA are fully dependent on the FPGA model.

TABLE II. POWER DISSIPATION FOR SYSTEM ARCHITECTURE BASED ON VARIOUS TOGGLE RATES USING POWERPLAY POWER ANALYSER

No.	Signals toggle rate			Power dissipation				Accuracy (Priority scale)
	Vectorless estimation	Default Toggle rate	VCD file	Total	Core dynamic	Core static	Input/Output	
1	All signals	-	-	200.44 mW	1.28 mW	154.97 mW	44.19 mW	3
2	Remaining signals	-	I/O signals	258.15 mW	57.66 mW	155.17 mW	45.31 mW	2
3	-	All signals with 12.5 %	-	198.86 mW	0.00 mW	154.97 mW	43.89 mW	5
4	-	Remaming signals with 12.5 %	I/O signals	199.39 mW	0.00 mW	154.97 mW	44.43 mW	4
5	Remaining signals	-	All available signals	235.46 mW	35.06 mW	155.09 mW	45.31 mW	1

**Priority scale: 1 = highest accuracy , 5 lowest accuracy

Thermal Power Dissipation by Block Type

	Block Type	Total Thermal Power by Block Type	Block Thermal Dynamic Power	Block Thermal Static Power (1)	Routing Thermal Dynamic Power	Block Average Toggle Rate (millions of transitions / sec)
1	JTAG	0.01 mW	0.00 mW	--	0.01 mW	6.250
2	PLL	0.00 mW	0.00 mW	--	0.00 mW	0.000
3	I/O	7.44 mW	1.31 mW	6.13 mW	0.00 mW	3.465
4	M4K	35.82 mW	35.82 mW	--	0.00 mW	0.000
5	Combinational cell	0.00 mW	0.00 mW	--	0.00 mW	0.000
6	Register cell	6.01 mW	6.01 mW	--	0.00 mW	0.000
7	Clock control block	15.83 mW	0.00 mW	--	15.83 mW	20.000

Fig. 9. Power consumption report by block type for system architecture produced by PowerPlay Power Analyser

V. CONCLUSION

In this paper, a power analysis of a Nios II processor-based system is carried out. The methodology to perform power analysis on the proposed system includes SoPC system integration, architecture design compilation, software program compilation using a processor tool chain, system simulation and power analysis. In this work, a peak detection algorithm is implemented into the embedded processor system for power analysis. Several configurations are used to carry out power analysis on the system architecture using the PowerPlay Power Analyser. Based on the power dissipation report, the estimated total power consumption is from 198.86 mW to 258.15 mW, while the core static power consumption is from 154.97 mW to 155.17 mW. Comparing the power consumption, the power analysis with a higher number of signal activities produced a more accurately estimated power consumption.

ACKNOWLEDGEMENT

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