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Design and Analysis of a Two-stage CMOS Op-amp using Silterra's 0.13 µm Technology

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***Abstract*— This paper presents the design and analysis of a high-gain, low-power, two-stage CMOS operational amplifier (op-amp) for a sigma-delta ADC. Op-amp topologies, such as folded cascade, telescopic and two-stage, are discussed in this paper. The theoretical and topological analyses of each design are highlighted in detail, including the trade-off among various parameters such as gain, noise, output swings and power consumption. The designs have been simulated using 0.13 um CMOS technology from Silterra (Malaysia) with Cadence EDA tools. From the simulation results, the two-stage amplifier gives better performance compared to other topologies, especially in terms of gain, output swing, slew rate and CMRR. The circuit is able to achieve 85.93 dB gain, a 1.1 V output swing, a 44.29 V/µs slew rate and a CMRR of 61 dB with a power supply voltage of 1.2 V.**

***Index Terms* — ADC, CMOS amplifier, folded cascade amplifier, two-stage amplifier, telescopic amplifier.**

I. Introduction

The analogue-to-digital converter (ADC) is an important building block in mixed signal applications. This circuit plays a significant role in ensuring the analogue signal is accurately represented in the digital domain. For this circuit, an operational amplifier (Op-amp) plays a significant role, since it determines the linearity and noise performance of the ADC.

The aim of this paper is to design and analyse various op-amp topologies that are suitable for use in ADCs. This paper is organized into five sections. Section 2 reviews the existing literature on two-stage amplifiers. In Section 3, the design methodologies for three op-amp topologies are discussed. Section 4 presents the simulation results of the proposed op-amp. Finally, Section 5 concludes the paper.

II. Literature Review

The paper in [2] presents a high resolution sigma-delta ADC used in medical applications to measure a low-frequency signal. In this ADC, a two-stage amplifier is used as one of the four op-amp topologies implemented in the system. As a result, the design has low power consumption while maintaining high performance.

In [3], a novel two-stage amplifier is discussed. This design implements the combination of a two-stage amplifier by adding a differential amplifier at the input and two transistors at the output of a two-stage amplifier with a voltage-to-current converter between the input and the output. The circuitry has large transconductance to achieve high gain bandwidth. It is suitable for designs where high frequency and low power consumption are the main criteria. The proposed two-stage amplifier is able to achieve a 25 ns settling time and a 50 V/µs slew rate with gain of 60 dB. This design reduces the power consumption by 10.5%.

Paper [4] discusses the design and analysis of a low-cost sigma-delta ADC. This circuit is to be used in a MEMS sensor interface circuit for biomedical application. The circuit implemented the first-order one-bit sigma-delta ADC using Silterra's 0.13 µm CMOS technology. This design gives better performance for weak signal acquisition by using a noise-shaping function which attenuates the signal bandwidth and pushes attenuated noise outside of the bandwidth.

Paper [5] discusses the design of a second-order sigma-delta ADC using 90 nm technology. This design implements a folded cascode amplifier as an integrator to provide high output swing and high sensitivity. This is achieved by having high gain with maximized output impedance.

The paper in [6] presents the design of an op-amp with a two-stage folded cascade structure using 0.18 µm CMOS technology. Since the design is targeted for use in portable medical instruments, the circuit is desirable in working with very low power consumption. This paper proposes a second-order sigma-delta which reduces the circuit complexity without using filter and buffering circuitry at the ADC's input.

III. Methodology

This section discusses the design of three op-amp topologies. First, the design of a two-stage op-amp will be discussed. This

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is followed by the description of a two-stage, telescopic op-amp and a folded cascade op-amp. In this work, the circuit is designed using Silterra's 0.13 µm CMOS technology, with a process parameter as shown in Table 1. In this work, simulations were performed using the Cadence Virtuoso Analog Development Environment software package [14].

Typically, an op-amp requires sufficiently high gain so that the closed loop transfer function is practically independent of the gain [7]. Fig. 1 shows the general two-stage CMOS op-amp block diagram. The circuit consists of two differential inputs followed by a common source at the second stage. The differential inputs provide the initial gain, while the second stage increases the gain by an order of magnitude and maximizes the output swing. The compensation is one method to increase the phase margin [1] and is required for stable closed-loop performance [9].

There are a few approaches to frequency compensation techniques to eliminate the effect of a right-half plane of zero, which can cause stability issues. These approaches include pole-splitting, a self-compensating capacitor and the inclusion of a transconductance stage to cancel the feedforward signal [13]. The compensation capacitor that is connected between the input and output nodes of the second stage causes the poles associated with them to split apart. This generates a non-dominant or dominant pole feedforward path that produces the right-half plane.

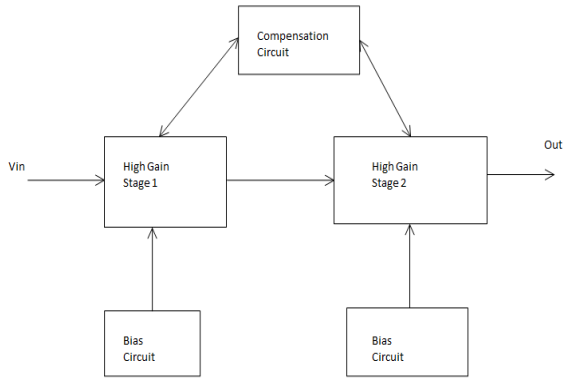

Fig. 1: Two-stage CMOS op-amp

Table 1: Process parameters for a two-stage amplifier design

Parameter	Value
Vdd	1.2V
Kn'	433.5uA/V
Kp'	120.27uA/V
Vtn	0.26V
Vtp	0.30V

Figs. 2-4 show three op-amp topologies. The two-stage amplifier topology seems to be more suitable compared to the other topologies, which suffered from low output swing and medium gain. Fig. 2 shows the schematic of the two-stage amplifier. The first stage of the two-stage amplifier consists of differential inputs which convert the input voltage to current. The second stage is a common source amplifier which converts the input voltage to current, while the M6 and M7 transistors convert current to voltage output, thereby acting as a current sink inverter. The DC gain for the two-stage amplifier can be expressed as:

$$Av = Av1 \times Av2 \quad (1)$$

Av1 is generated by the fully differential amplifier at the first stage, while Av2 is the gain for the source follower at the second stage. The DC gain can be represented as:

$$Av = Gm \times Rout \quad (2)$$

where Gm is the transconductance of the input network and Rout is the effective output resistance. Table 2 summarizes the dimension for each transistor for the two-stage amplifier. The two-stage amplifier DC gain is given as [2]:

$$A_d = g_{m1st}(r_{01} \| r_{04}) \bullet g_{m2nd}(r_{06} \| r_{07}) \quad (3)$$

Fig. 3 shows the schematic of the telescopic amplifier. Compared to the other topologies, this topology gives the highest power efficiency due to its load compensation [2], and it produces high gain [10 and 11]. At a reduced power supply voltage, the telescopic amplifier gives a small output swing. Thus, it is usually suitable for use in feedforward sigma-delta topologies, when a high output swing is not important [12]. Table 3 shows the dimensions for each transistor according to W/L for the telescopic amplifier. The telescopic amplifier DC gain is given as [10]:

$$A_d = g_{m1st}(g_{m3} r_{03} r_{05} \| g_{m2} r_{02} r_{08}) \quad (4)$$

Fig. 4 shows the schematic of folded cascode amplifier. The circuit provides higher voltage swing compared to the telescopic amplifier due to the overdrive voltage at the tail of the current source [2]. Table 4 shows the dimensions for each transistor for a folded cascode amplifier. The folded cascode amplifier DC gain is given as [2]:

$$A_d = g_{m1st}(g_{m4} r_{ds4} r_{d2} \| (r_{ds6} \| r_{ds7}) \quad (5)$$

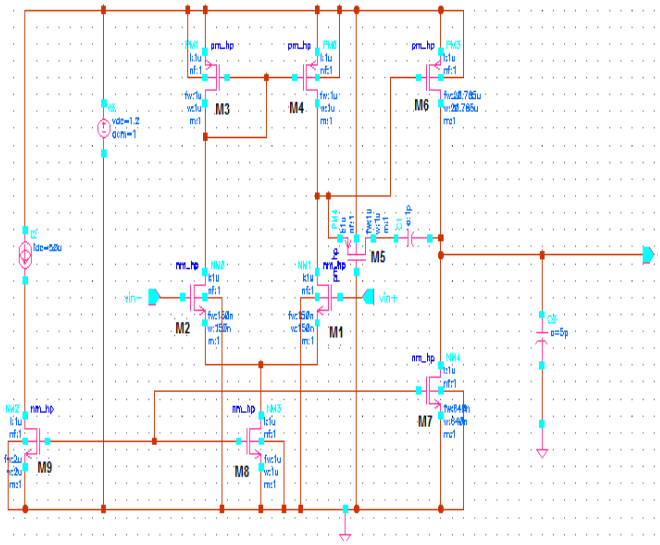

Fig. 2: Op-amp topologies: two-stage

Table 2: Design results of each transistor dimension for the two-stage amp

Transistor	W/L
M1	4u/1u
M2	4u/1u
M3	10.5u/1u
M4	10.5u/1u
M5	1u/1u
M6	22u/1u
M7	17u/1u
M8	18u/1u
M9	18u/1u

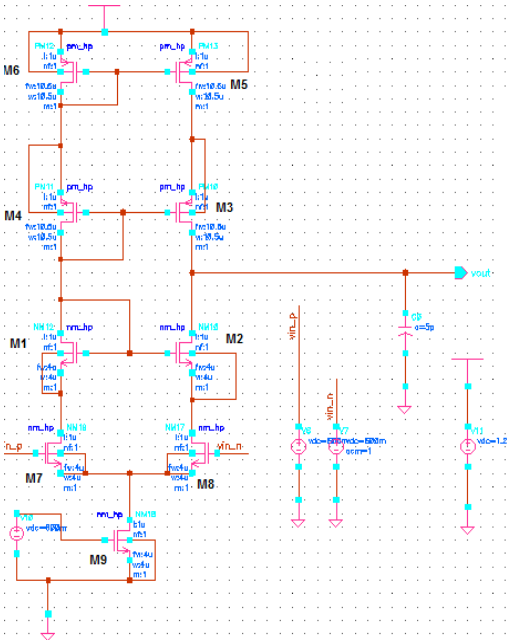

Fig. 3: Op-amp topologies: telescopic

Table 3: Design results of each transistor dimension for the telescopic amp

Transistor	W/L
M1	4u/1u
M2	4u/1u
M3	10.5u/1u
M4	10.5u/1u
M5	10.5u/1u
M6	10.5u/1u
M7	4u/1u
M8	4u/1u
M9	4u/1u

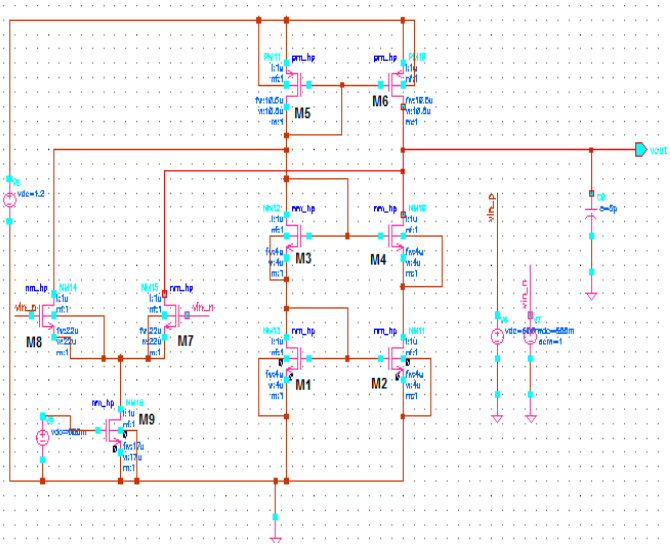

Fig. 4: Op-amp topologies: folded cascode

Table 4: Design results of each transistor dimension for the folded cascode amp

Transistor	W/L
M1	4u/1u
M2	4u/1u
M3	4u/1u
M4	4u/1u
M5	10.5u/1u
M6	10.5u/1u
M7	22u/1u
M8	22u/1u
M9	17u/1u

IV. Results & Discussion

This section discusses the simulation results for the two-stage, telescopic and folded cascode op-amps. The simulation results for the two-stage amplifier gain are shown in Fig. 5. From the figure, the circuit is able to archive a maximum gain of 85.93 dB with a frequency bandwidth of 3.9 KHz. Fig. 6 shows the frequency response for the telescopic amplifier. From the figure, the circuit is able to obtain 29.67 dB with a frequency bandwidth of 3.8 KHz. The folded cascade op-amp performance is depicted in Fig. 7. Based on the simulation results, a maximum gain of

49.3 dB is achieved for the folded cascade with an 84 KHz bandwidth.

Table 5 shows the performance comparisons among the various op-amp topologies. From the table, the two-stage op-amp provides the highest gain (85.93 dB), the high output swing (close to VDD), a high slew rate (44.29 V/uμ) and better CMRR (61 dB) compared to the other topologies. However, the two-stage amplifier exhibits higher power consumption. Therefore, the two-stage topology is more suitable for applications where high gain and high output swing are the main concern.

Table 6 compares the performance of two-stage amplifiers implemented in a sigma-delta ADC as discussed in [10, 15 and 16]. From the table, the two-stage op-amp that is designed in this work gives better performance in terms of gain, bandwidth and slew rate, which are the important parameters for designing a sigma-delta ADC [4].

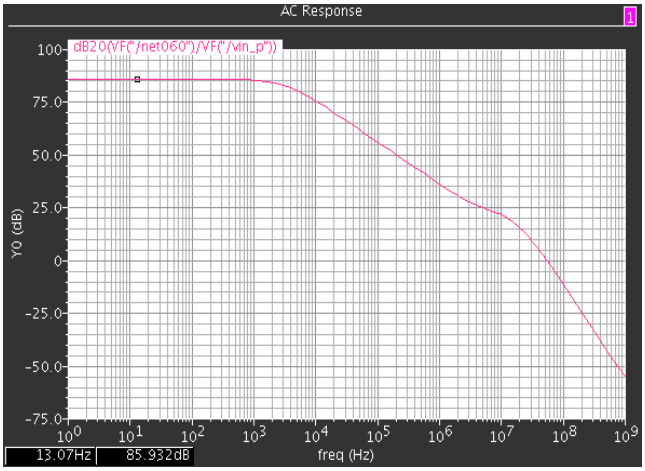

Fig. 5: Results of AC analysis for the two-stage op-amp

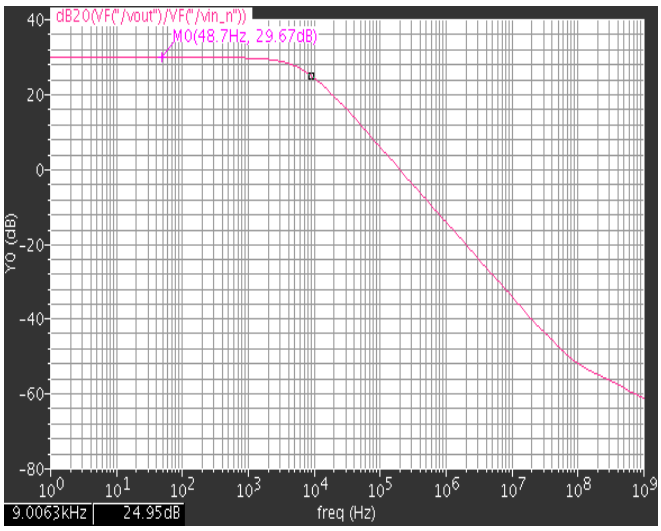

Fig. 6: Results of AC analysis for the telescopic op-amp

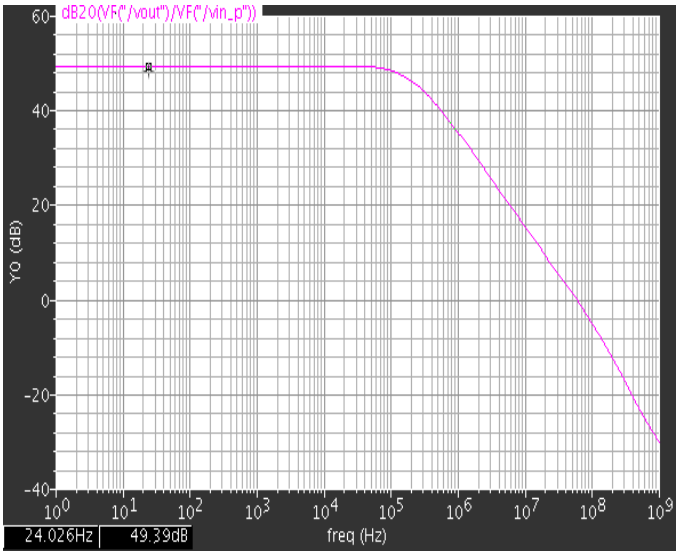

Fig. 7: Results of AC analysis for the folded cascode op-amp

Table 5: Comparison of the performance of various op-amp topologies

Parameter	Two-Stage	Telescopic	Folded Cascode
Power Supply	1.2V	1.2V	1.2V
Gain	85.93dB	29.67dB	49.3dB
Output Swing	1.1V	0.7V	0.7V
Power Consumption	109.07uW	16.25uW	212.57uW
Slew Rate	44.29V/us	35.30V/us	2.71V/us
CMRR	61dB	56.78dB	52.71dB
Unity Gain Bandwidth	55MHz	394.6KHz	58MHz
Area	10umx39um	8umx14.5um	13umx32.5um

Table 6: Comparison of the performance of various op-amp topologies

Parameter	[10]	[15]	[16]	*This work*
Power Supply	0.9V	±1.5V	±1.2V	1.2V
DC Gain	54dB	60dB	38dB	85.93dB
Output Swing	0.77V	±1.5V	±1.2V	1.1V
Power Consumption	1.75uW	0.36mW	N/A	109.07uW
Slew Rate	2.40V/us	50V/us	0.5V/ms	44.29V/us
Technology	65nm	0.35um	0.13um	0.13um
Unity Gain Bandwidth	7.8MHz	80MHz	2.735MHz	55MHz

V. Conclusion

This paper discussed the design of three op-amp topologies. The circuit was simulated and the performance of each topology was compared. From the simulation results, the two-stage op-amp appears a good candidate for use as an integrator in a sigma-delta ADC as compared with the other topologies. The simulation results show that the two-stage op-amp meets the required performance, with high gain (85.93 dB), a high output swing (1.1 V), a high slew rate (44.29 V/μs) and better CMRR (61 dB). In the next phase of this work, we will focus on the analysis of circuit techniques to reduce the power consumption in the two-stage op-amp.

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