Design and Analysis of a Two-Stage OTA for Sensor Interface Circuit

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***Abstract*—This paper discusses the design of an operational transconductance amplifier (OTA) circuit for use in a capacitive sensor interface circuit. The OTA converts a differential voltage input into the current as part of a switched capacitor integrator module. In this paper, a two-stage OTA is proposed which has high gain, high output swing and low noise. The circuit was implemented using 0.13 µm Silterra CMOS technology and simulated using the Mentor Graphic Design Architect software package. The results show that the OTA is able to achieve 74 dB gain and 20 KHz bandwidth when operated using a 2.5 V power supply, with a total power consumption of 1.3 mW.**

Keywords— Operational transconductance amplifier (OTA); Two-stage amplifier, Capacitive sensor interface circuit.

I. INTRODUCTION

Sensors are widely used in today's applications, such as in biomedical and environmental monitoring and instrumentation [1, 3]. These sensors are used to detect various signals, such as light, position and movement. In biomedical applications, smart devices combine several sensors into a single circuit to detect various physiological signals, such as blood-sugar level, heartbeat rate and the presence of any toxic agents [2-3]. To combine these sensors efficiently, they must be connected to a multi sensor interface circuit that can support a variety of sensors using a single circuit [4]. Thus, such a circuit must be able to support a wide variety of sensor types, such as voltage, current, capacitance and resistance, and must also be able to provide a useable signal for further processing and communication with the microsystems' controller [2].

Among various sensor types, capacitive sensing has the capability to detect a variety of parameters, such as proximity detection, position detection, pressure detection and microelectromechanical system [5-6]. A capacitive sensor interface circuit is needed for capacitive-based sensing and is useful in microsystems applications due to its low power and high sensitivity [3]. The basic building block of a capacitive sensor interface circuit is the switched capacitor integrator. Most switched capacitor integrators utilize a two-stage amplifier to produce high gain that cannot be obtained using a single-stage amplifier [18].

This paper discusses the design of an operation transconductance amplifier (OTA), which is the basic building block of a switched capacitor integrator. While there are many types of OTAs available in the literature, this work focuses on the two-stage OTA, since the circuit can produce the required output current and gain for capacitive sensing applications [6-8, 10].

This paper is organized as follows. Section 2 discusses various types of OTA available in the literatures. The OTA design methodology is elaborated in Section 3. Section 4 highlights the experimental results obtained in this work. Finally, Section 5 concludes this paper.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) TOPOLOGY

In this section, three types of OTA will be discussed and their performance will be compared. These topologies comprise two-stage, telescopic and folded cascade OTAs. The advantages and disadvantages of each topology will be highlighted.

A. Two-stage OTA

The two-stage OTA circuit is shown in Fig. 1. This circuit consists of eight main transistors, with each transistor performing a specific function. Transistors M1 and M2 are the input for the first stage (differential amplifier), which converts voltage signals into current. Transistors M3, M4, M5 and M8 act as a current mirror, while transistors M6 and M7 form the second-stage amplifier. This topology has the advantage of providing higher gain because the second stages provide higher output voltage swing. The disadvantage of this circuit is that it consumes more power

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and gives negative power supply rejection (PSR) at higher-frequencies [13].

B. Telescopic OTA

Fig. 2 illustrates the telescopic OTA. This structure is called a 'telescopic cascade op-amp' because the transistors are cascades between the power supplies in series and the transistor in the differential pair. This design increases the output impedance and voltage gain due to the cascade transistor and has low power consumption. Its output swing is very small and it is not suitable for applications where the input and output need to connect directly, since this reduces its linearity range [13-14].

C. Folded cascade OTAs

The folded cascade OTA is shown in Fig. 2. This circuit is called 'folded cascade' because it folds down *n*-channel cascade active loads of a differential pair and replaces the input transistor with a *p*-channel MOSFETs [11]. The PMOS transistors M9 and M10 are used as a differential input stage to charge the Wilson mirror (M5, M6, M7 and M8). The NMOS transistors M11 and M12 provide the DC bias voltages to transistors M5 through to M8. This topology improves the output swing compared to other topologies because it consists of fewer transistors at the output stage. In addition, this topology has a better high-frequency power supply rejection ratio (PSSR) and a wider frequency response compared to the two-stage OTA. However, this topology consumes more power and contributes to greater noise [12-14].

Table 1 summarizes the comparison of the different OTAs. Based on the table, the two-stage OTA has higher gain compared with the other topologies. This comes with lower speed compared to the other topologies. Among these three circuits, the folded cascade has a higher speed compared with the others. In this work, as part of a switch capacitor circuit for a capacitive sensor interface circuit, the two-stage OTA is chosen due to its high gain, which is critical for this type of application. In the next section, the design of this two-stage OTA is discussed in detail.

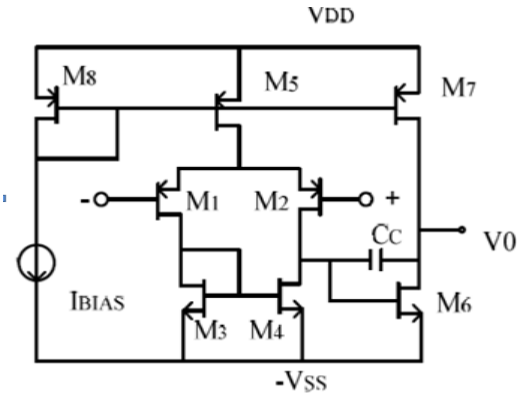

Figure 1. Two-stage OTA [16].

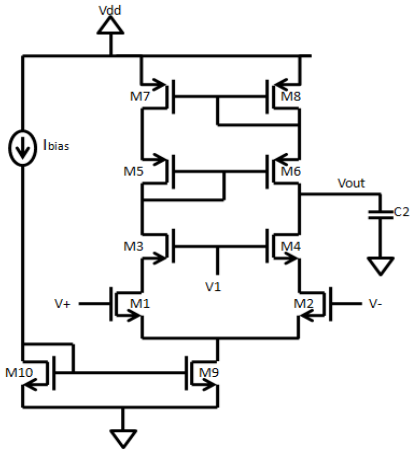

Figure 2. Telescopic OTA [11].

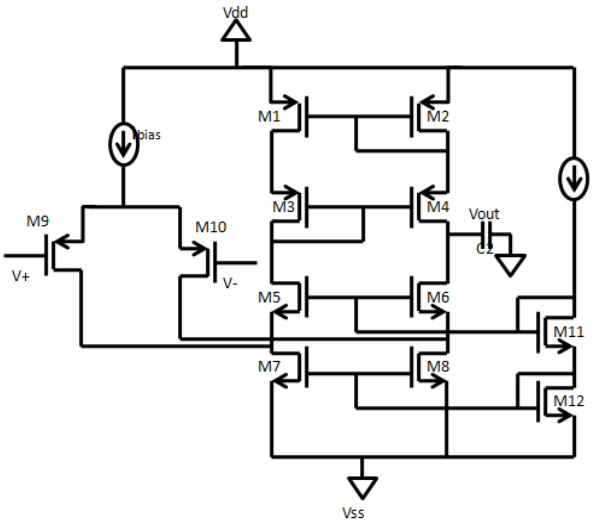

Figure 2. Folded cascade OTA [11].

TABLE 1: COMPARISON OF DIFFERENT TOPOLOGIES [13]

Topology	Gain	Output Swing	Speed	Power
Two-stage	High	Highest	Low	Medium
Telescopic	Medium	Medium	Highest	Low
Folded cascade	Medium	Medium	High	Highest

TABLE II:OTA SPECIFICATION

Specifications	Value
Differential gain , Av (dB)	≥70
Gain bandwidth product , GBW (MHz)	≥20KHz
Phase margin, PM (degree)	≥60
Slew Rate, SR (V/µs)	≥40
Average Power consumed, P(mW)	<5
Power source, Vdd (V)	2.5
Output load capacitance , CL (pF)	3
Compensation Capacitance , Cc (pF)	1.1
Input offset voltage, Vos (V)	10mV

III. METHODOLOGY

In this section, the design of the two-stage OTA, as shown in Fig. 1, is discussed. The initial specification of the design is set as shown in Table II. We use the gm/Id methodology to determine the transistor sizing (W/L) for each transistor in the OTA circuit [16]. The design started by estimating the value of the compensation capacitor, Cc. For a 60^o phase margin, the following equation is used:

$$Cc = 0.22 \times CL >> Cc = 3pF \quad (1)$$

Next, the bias current, I_{bias}, was determined based on the slew rate specification. I_{bias} = 80 µA was estimated as given by the following equation:

$$I_{bias} = SR \times Cc \quad (2)$$

When Vgd3 = 0, the transistor M3 is in a saturation region. As the systematic offset condition provides that the drain voltage of M4 is equal to the drain voltage of M3. M2 and M1 have same value. Next, the transistor sizing for M8 is determined from Vgd8 = 0, where it operates in a saturation region. The size of transistors M5 and M6 will be calculated next using the current mirror concept with transistor M8.

In this design, the transistor length is set to L = 1 µm. Based on the above discussion, $W_1 = W_2$, $W_3 = W_4$ and $W_5 = W_8$. Thus, I_1, I_5 and I_7 can be expressed according to equations (3) to (5). In this design, we used a cascade current mirror (M9-M13) as a biasing circuit for M8.

$$I_5 = ((W_5/L_5)/ (W_8/L_8)) \text{ x } I_{bias} \quad (3)$$

$$I_7 = ((W_6/L_6)/ (W_8/L_8)) \text{ x } I_{bias} \quad (4)$$

$$I_1 = I_5/2 = 1/2 ((W_5/L_5)/ (W_8/L_8)) \text{ x } I_{bias} \quad (5)$$

TABLE III: OTA PARAMETER VALUE.

Devices	Value	
	W	L
M1,M2	10µm	1µm
M3,M4	20µm	1µm
M6	200µm	1µm
M7	100µm	1µm
M8,M5	40µm	1µm
M9,M10,M11,M12,M13	25µm	1µm
Supply voltage	Vdd=2.5V	
Load Capacitance (CL)	3pF	
Compensation Capacitor	1pF	
Bias current, I_{bias}	70µA	

IV. RESULTS AND DISCUSSION

Fig. 4 shows the finalized schematic of the two-stage OTA, while Table III shows the final transistor size for the two-stage OTA. The circuit has been designed using the Silterra 0.13 µm CMOS technology and simulated using the Mentor Graphic Design Architect software package. Various circuit characteristics are simulated for the OTA, such as the gain, phase margin, power consumption, slew rate and input range common mode (ICMR).

Fig. 5 shows the simulated AC analysis of the two-stage OTA. Based on the figure, a 62^o phase margin, 74 dB gain and 20 KHz bandwidth are obtained. Fig. 6 shows the slew rate simulation results. It is measured by applying a step signal ranging from 0.1 V to 1.4 V. From the figure, the value for the slew rate is 47.90 V/µs and the setting time is 19.69 ns.

Fig. 7 shows the result for the ICMR. These characteristics are measured using a unity gain configuration. A DC transfer sweep is plotted and the linear parts of the curve show the input common mode voltage range at around 0.3 V to 2.5 V. Fig. 7 shows the results for the voltage output swing. It is simulated in DC analysis using the ELDO simulator. The output swing can be determined from the saturation at 2.4 V. Table IV summarizes the overall characteristics of the designed OTA.

Table V compares our work with other existing work in the literature. From the table, our design is able to achieve higher gain in comparison. This comes at the cost of higher power consumption and a smaller gain bandwidth as compared to the literature.

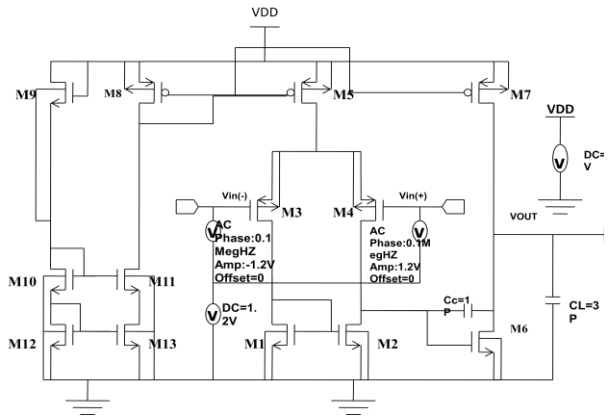

Figure 4. Two-stage OTA simulation circuit.

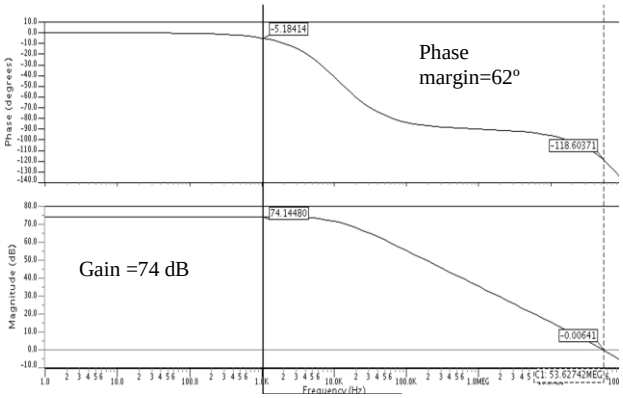

Figure 5. Output of the AC analysis.

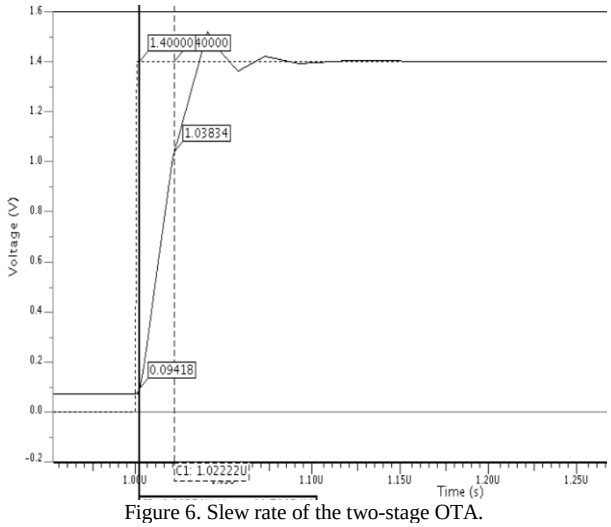

Figure 6. Slew rate of the two-stage OTA.

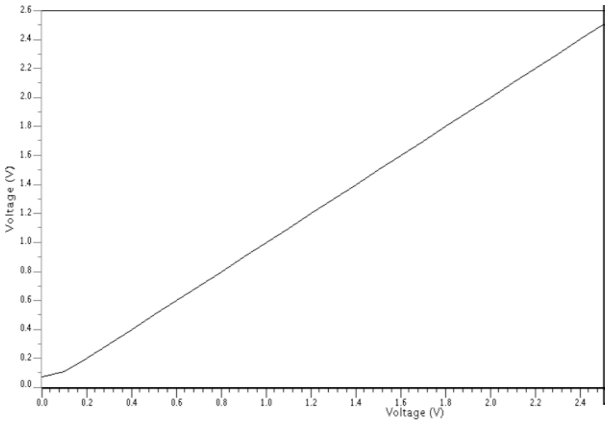

Figure 7. ICMR two-stage OTA.

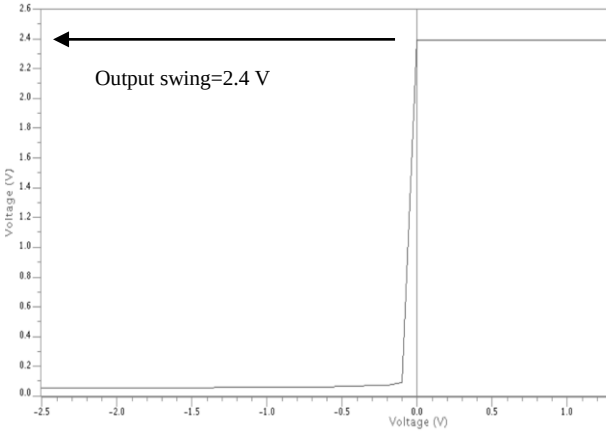

Figure 8. Output swing of the two-stage OTA.

TABLE IV: SIMULATION RESULTS FOR THE TWO-STAGE OTA

Specifications	**Value**
Technology	Silterra0.13µm
Power supply (V)	2.5
Differential gain, AV (dB)	74
Gain bandwidth product,GBW	20khz
Phase margin, PM (degree).	62º
Slew rate, SR (V/µs)	47.90
Average power consumed (mW)	1.3
ICMR (V)	0.2<ICMR>2.5
Output swing (V)	2.4

TABLE V:COMPARISON OF VARIOUS OTA TOPOLOGIES

Specifications	[17]	[19]	This work
Technology	0.18µm	0.35µm	0.13µm
Topologies	Folded cascode	Telescopic	Two-stage
Power supply (V)	1.8	2.5	2.5
Differential gain, AV (dB)	68.53	40	74
Gain bandwidth product,GBW (Hz)	0.2M	60M	0.1K
Phase margin, PM (degree).	66º	70º	62º
Average power consumed (mW)	0.04	0.0026	1.3

V. CONCLUSION

A capacitive readout circuit is important in multi-sensor interface circuits. The aim of this work has been to design a two-Stage OTA which forms the basic building block of a capacitive readout circuit. The circuit was designed using 0.13 µm Silterra CMOS technology and achieved 74 dB gain, a ~48 V/µs slew rate, 1.3 mW power consumption, a 62º phase margin, and 20 KHz gain bandwidth. In the next phase of this work, the circuit will be integrated with other components to form a capacitive interface in a multi-sensor interface circuit for a bio-analyzer

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