Circuit Architectures Reviews for Portable ECG Signal Analyzer

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***Abstract*- This paper discusses the circuit comparison of the electrocardiogram (ECG) heart rate detector for wearable biomedical devices. In this work, the QRS complex is used to calculate heart rate, representing the main component of the ECG signal. In order to achieve a high level of accuracy by the detector, the measured ECG signal must be free of noise. Typically, such noise originates from power line interferences and baseline wandering. To eliminate these noises, the ECG signal must be processed using the signal processing method. The ECG detection process can be divided into a preprocessing stage, which eliminates noise from the raw ECG signal, and the feature extraction stage, which extracts the QRS complex for heart rate calculation. Based on our analysis, the trade-off between complexity and accuracy in ECG signal architecture is important when designing a high-efficiency system.**

Keywords: ECG; QRS; Preprocessing; Feature Extraction

I. INTRODUCTION

Today, personalized health monitoring devices are important for intensive care and diagnostic assessment. There is a growing demand for high quality health monitoring systems to provide better healthcare services, since the lifestyle of an individual is affected by the environment surrounding them.

An electrocardiogram (ECG) is a biomedical signal that comes in the form of an electrical current generated by the heart, and that can be detected at the surface of the body [1]. ECG monitoring and analysis becomes essential for the early diagnosis of cardiac disease. Therefore, many devices are implemented to calculate heart rate based on an ECG signal to determine the user's condition. An unusual heart rate pattern in a patient might reflect that the patient is suffering from cardiac disease. A typical ECG signal, as shown in Fig. 1, is composed of a P wave, Q, R, S points, and a T wave in sequence. A combination of Q, R, S points—known as a QRS complex—is the main component and is commonly used to calculate heart rate in medical fields since it has higher energy and a greater amplitude than other components within the ECG signal. However, the ECG signal is usually contaminated by noise, particularly due to power line interference and baseline wandering [2]. Thus, noise suppression needs to be implemented to eliminate noise before extraction of the QRS complex for further processing.

To allow continuous monitoring of the ECG signal, the device should be wearable or implantable into the body. Thus, it needs to be small and have the fewest disturbances possible from other human bodily signals and surrounding interference. However, high detection reliability and power consumption becomes an issue when the device is built in a smaller size [3]. For this portable device, high detection accuracy requires a large computational load and high energy consumption. As a result, the device battery would not last long enough for continuous ECG monitoring. Thus, the monitoring device must be optimized for accuracy of detection and lowest possible energy consumption.

This paper highlights several popular designs for an ECG detector that have been proposed in the relevant literature. Various aspects of these devices will be discussed to compare the best approach. Section II will review the existing methods of implementing an ECG detector, whilst section III makes a comparison of performance in term of power consumption, size, accuracy, technology, and supply voltage. Finally, Section IV concludes this paper.

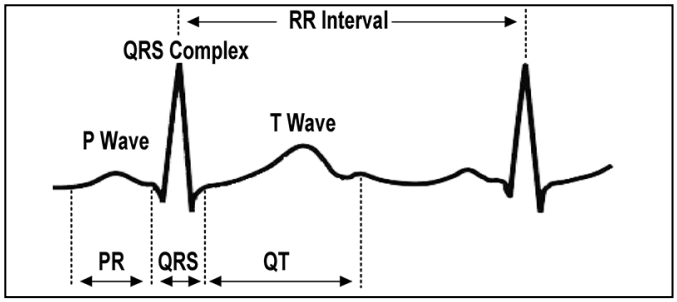

Fig. 1. ECG Signal [8].

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II. LITERATURE REVIEW

The author in [4] proposed an application-specific integrated circuit *(*ASIC) for ECG implementation as shown in Fig. 2. The architecture is said to be the first real-time form of QRS detection to implement the algorithm developed by Pan and Tompkins in 1985 [5]. The algorithm has been widely used for QRS detection purposes up to the present, due to its simplicity and robustness in relation to hardware implementation. The band-pass filter, which consists of a low pass and high pass filter, eliminates 60 Hz interference and baseline wandering. The signal is differentiated at the next stage to find the QRS slope information. The squaring process is then applied to make all data points positive and to emphasize the higher frequencies. The moving window integrator adds a further discrimination effect to the QRS complex before proceeding to a peak detection stage.

According to the architecture shown in Fig. 3, the authors of [6] implemented the proposed ECG signal-processing scheme in ASIC for long-term cardiac monitoring. Multiple functions including baseline-drift removal, noise suppression, QRS detection, heart rate prediction and classification, and clean ECG reconstruction were included. Decomposition was executed by wavelet transformation to distribute the incoming noisy ECG into different scales with different bandwidths. Power line noise was suppressed by the noise suppression module based on outputs from scales 1 to 4, while baseline drift was removed from a scale of 7 to 8. QRS detection was performed based on the adaptive threshold method, which calculates the threshold for every specific window. An adaptive prediction scheme was proposed to classify different individual statuses depending on heart rate.

The authors of [7] proposed an ECG acquisition and monitoring system with the architecture shown in Fig. 5. Here, the digital ECG signal processing (DSP) back-end consists of a discrete wavelet transform (DWT), de-noising block, and QRS detection block. DWT performs a four-scale decomposition to extract the characteristic points of the ECG. De-noising is performed by multiplication of the adjacent outputs from the wavelet decomposition block, with calculation of the threshold and imposition on multi-scale products to identify the important features. The QRS detection block is performed using an adaptive threshold method. To locate the QRS position, this adaptive threshold scheme calculates the standard deviation on every window with a specific number of samples on the outputs from a noise suppression block.

The authors in [8] proposed an architecture design as shown in Fig. 5. The proposed architecture consists of three major blocks: wavelet decomposer, noise detector, and QRS complex detector. A multi-scaled product inside the QRS complex detector reconstructs the ECG data by selecting outputs from the wavelet decomposition block according to noise information from the noise detector. A soft-threshold algorithm in the complex detector block increases the threshold value for every 200 ms following a QRS complex detection to avoid the possibility of false detection on the T point that appears after the QRS complex.

The architecture [9] in Fig. 6 proposes a QRS detection processor integrated with an ADC and wireless controller to perform real-time verification. Wavelet transform, feature extraction, and decision-making stages are the blocks used to optimize the detection accuracy of the QRS complex. Wavelet transform is applied to obtain a smooth derivative of the input signal. The R peak is transformed into a modulus maxima pair (positive-maximum-negative-minimum). The feature extraction stage is accomplished by zero-crossing detection, peak detection, and threshold adjustment. It indicates the zero-crossing point by identifying the wavelet transform output peak—either upward or downward—and the threshold to categorize the peak as a signal or noise peak. Finally, the decision stage is realized by two finite state machines (FSM) that locate the QRS complexes.

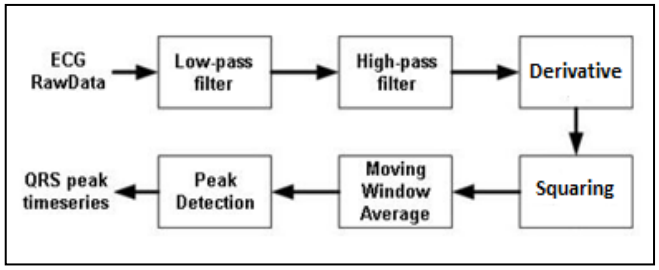

Fig. 2. Architecture in [4].

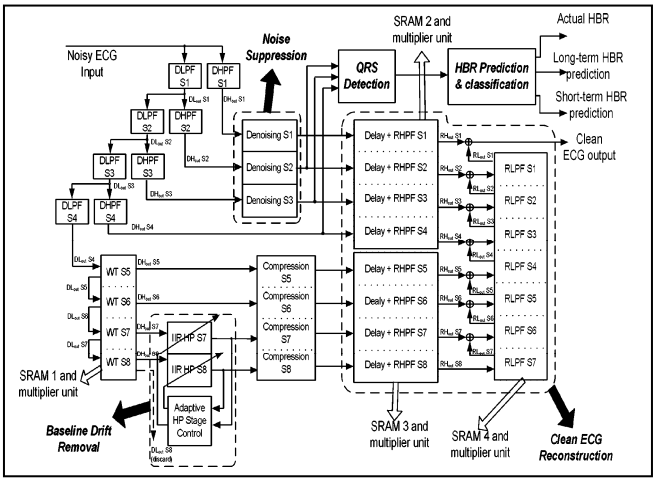

Fig. 3. Architecture in [6].

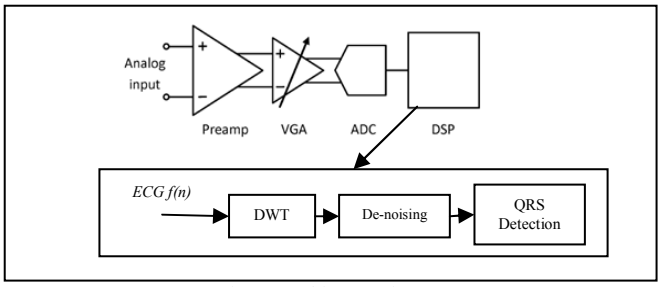

Fig. 4. Architecture in [7].

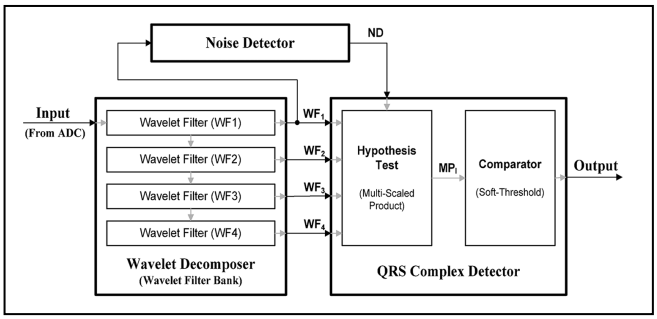

Fig. 5. Architecture in [8].

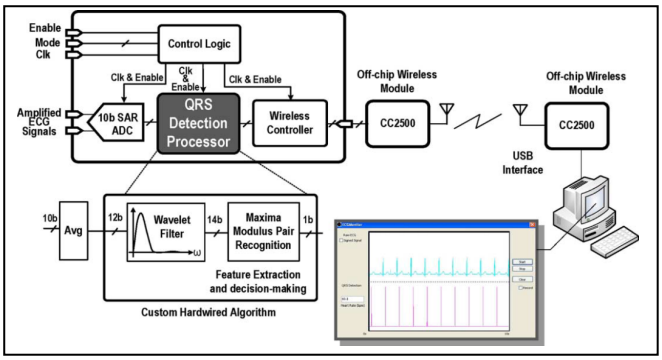

Fig. 6. Architecture in [9].

III. RESULT AND DISCUSSION

Based on the literature discussed in the previous section, the ECG signal requires two stages: preprocessing and feature extraction. The preprocessing stage includes baseline wandering removal and power line interference suppression. The feature extraction stage extracts the characteristics of the ECG data and performs QRS complex detection. These outputs are essential for diagnosing a cardiac condition.

Among the various architectures that have been discussed, wavelet transform is a common technique implemented in the preprocessing stage. The advantage of wavelet transform is its ability to decompose the incoming ECG signal into different scales that represent the signal in different bandwidths. Furthermore, the wavelet transform-based architecture has low computational complexity and a simple digital circuit implementation using the FIR filter approach [6-9].

Table 1 compares the overall performance of the architectures in [4, 6-9] in terms of detection accuracy, size, power consumption, technology, operating frequency, and supply voltage. Based on the comparison in Table 1, the architecture in [8] provides the lowest detection error rate (DER) with 0.196%. The implemented soft-threshold algorithm in [8] is able to change the threshold for QRS detection to a higher value for every 200 ms after a QRS complex is detected. This solution avoids the possibility of a T point signal detection that comes after the QRS complex.

TABLE 1. COMPARISON OF QRS DETECTOR ARCHITECTURES

Architecture		[4]*	[6]	[7]	[8]	[9]
CMOS Process (µm)		0.18	0.18	0.18	0.35	0.35
Supply Voltage (V)		N/A	1	1.1	3	1.8
DER (%)		4.99	0.35	0.35	0.196	0.99
Frequency (Hz)		500	32K	32K	1K	300
Area (mm^2)	ADC	N/A	N/A	4.25	1.61	0.096
	Processor	0.68	3	1.2	1.2	1.11
Power (µW)	ADC	N/A	N/A	79.6	5.42	2.36
	Processor	2.21	29	9	13.6	0.83

*Detection Error Rate results are based on 5 records from MIT-BIH database

TABLE 2. COMPARISON OF QRS DETECTOR ARCHITECTURES for 0.18µm CMOS CIRCUIT (NORMALIZED)

Architecture	[4]*	[6]	[7]
CMOS Process	0.18	0.18	0.18
Supply Voltage	N/A	1	1.1
Normalized DER (A)	1.0	0.07	0.07
Normalized Total Area	1.0	4.4	8.0
Normalized Frequency (B)	1.0	64.0	64.0
Normalized Total Power (C)	1.0	13.1	40.1
Architecture Energy Efficiency (C/B)	1.0	0.2	0.6
Overall architecture performance [(C/B)*A]	1.0	0.01	0.04

TABLE 3. COMPARISON OF QRS DETECTOR ARCHITECTURES for 0.35µm CMOS CIRCUIT (NORMALIZED)

Architecture	[8]	[9]
CMOS Process	0.35	0.35
Supply Voltage	3	1.8
Normalized DER (A)	0.2	1.0
Normalized Total Area	2.3	1.0
Normalized Frequency (B)	3.3	1.0
Normalized Total Power (C)	6.0	1.0
Architecture Energy Efficiency (C/B)	1.8	1.0
Overall architecture performance [(C/B)*A]	0.35	1.0

Since each literature uses a different CMOS fabrication technology, to provide a fair comparison for each architecture Table 2 and 3 show the normalized value of the performance metrics for the 0.18µm and 0.35µm CMOS processes, respectively. Furthermore, since power consumption is directly proportional to frequency, the metric C/B reflects the architecture energy efficiency, while (C/B)*A reflects the overall performance of the architecture when accuracy is taken into account.

Based on Table 2, for the 0.18µm CMOS process, architecture [4] provides the most energy-efficient implementation whereas the best overall performance is provided by architecture [6]. For the 0.35µm CMOS process, architecture [9] gives the more energy-efficient architecture, while an overall strong performance is provided by architecture [8].

Based on the observations from Table 2 and 3, it is clear that there exists a tradeoff between accuracy and circuit energy consumption when designing an ECG data analyzer. This is because, the more computation is performed to process the signal, the accuracy of the detector tend to be higher. While for portable devices minimizing energy consumption is the main target, this must be achieved without sacrificing the accuracy of the analyzer. In the next stage of this research, the optimum trade-off between accuracy and energy consumption will be studied in detail.

IV. CONCLUSION

In this paper, comparisons of five existing QRS detectors have been made. Overall, the raw ECG signal has to be preprocessed to eliminate baseline wandering and power line interferences, so that the QRS detection accuracy can be enhanced. Several wavelet-based architectures have been proposed in recent years due to their low complexity and high efficiency in hardware implementation using a FIR filter approach. To achieve a high detection accuracy, the system requires high computational load, which consumes more power. Thus, the trade-off between hardware efficiency and power consumption must be considered in order to achieve an optimum system performance. In the next phase of this work, a case study of [8] will be focused upon since this provides the highest detection accuracy.

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