Standard Cell Library Development

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Abstract: The goal of this paper is to discuss the development of standard cell library creation by Library Development Group, Microelectronics Lab, MIMOS. This involves in creating new design rule, layout design, simulation and verification of each standard cell and finally characterization of all cells for timing and functional properties. The library implemented in this work is designed base on the technology develop by MIMOS Wafer Fab process.

1.0 Introduction

The key success factor for the rapid growth of the integrated system is the use of ASIC library for various system functions. It consists of predesigned and preverified logic blocks that help designers to shorten product-development time and manage the complexity of a chip having millions of logic gates or more.

Standard cell library contains a collection of components that are standardized at the logic or functional level. It consists of cells or macrocells based on the unique layout that designers use to implement the function of their ASIC. The economic and efficient accomplishment of an ASIC design depends heavily upon the choice of the library. Therefore it is important to build library that full fills the design requirement.

MIMOS, through its Semiconductor Technology Program has acquired the library for both 1.0μ CMOS and 0.5μ BiCMOS. The former has successfully been used to design several applications such as Pesona, a 16-bit RISC processor; and SECRET, an encryption engine. Currently, MIMOS is expanding its technology to develop 0.8μ CMOS library, which consists of basic standard cells such as logics and registers. In the following section, we will present the flow of an on-going work for the development of cell library in MIMOS.

2.0 Design Requirement

Since at the early design stage, the cells are targeted to meet certain function and performance. Typically, the cells will be designed to be either area-optimized or speed-optimized version. The former uses minimum sized transistors to achieve the smallest area while the latter uses larger transistors to provide good driving capability. More complex logic function can be added to the library by combining the basic logic function.

The cells are verified for their performance characteristics. The setup, hold, minimum cycle time, enable and disable times provided with simulation models, has to be verified through either circuit simulation or from actual hardware test.

In addition, various aspects of variation due to fabrication process have to be considered, such as:

a. temperature, voltage and process
b. best and worst-case timing

Thus, the cells need to be characterized at different condition that will reflect behavior of the cells in real application.

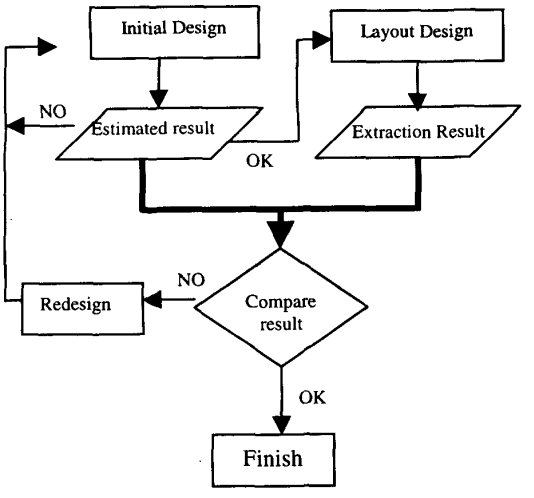

Figure 1: The flow chart for standard cell design

3.0 Standard cell Design

The Figure 1 shows the design flow for the standard cell. The design starts with the circuit topology of the cell either using schematic or netlist entry. At this stage, the width of NMOS, *Wn*, and PMOS, *Wp*, of the transistor are optimized. *Wp* and *Wn* are selected to meet design specifications such as power dissipation, propagation delay, noise immunity and area [1].

The value of *Wp* and *Wn* are determined by:

a. DC switching point , which is approximately 50% of the *Vdd*.
b. drive capability of the cell, i.e. the number of fanout that the cell can drive.

For an approximate same rise and fall time, *Wp* is normally three times wider than *Wn*. A circuit simulator is used to determine the switching point.

4.0 Layout methodology

If the circuit functions as expected, the physical design for the cell will be created and the parasitic value such as capacitance is back-annotated to obtain the actual delay associated with the interconnect.

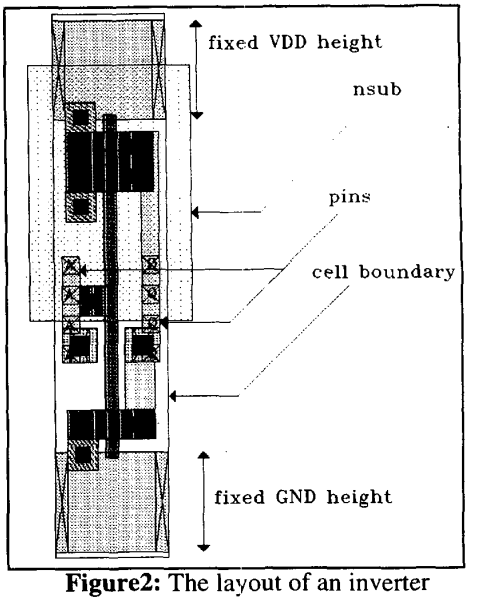

Figure2: The layout of an inverter

Figure 2 shows the layout of an inverter. The layout uses the standard cell technique [2], where signals are routed in polysilicon perpendicular to the power. This approach result in a dense layout for CMOS gates, as the vertical polysilicon wire can serve as the input to both the NMOS and PMOS transistor. The row of n-transistor and p-transistor separated by a distance specified in the design-rule separation between n- and p- active area [3]. Power and ground busses traverse the cell at the top and bottom respectively. The internal area of the cell is used for routing the transistors of specific gates. To complete the logic gate, connections is made in metal, where metal1 routed horizontally and metal2 vertically.

5.0 Characterization process

The cells are simulated to ensure proper functionality and timing. The results from the initial design and extracted values are compared. A BSIM model is used to simulate the nominal process from the fab.

Measurement of all delay times are at 50% to 50% *Vdd* values. All rise/fall times are 10% to 90% *Vdd* values [3]. To obtain realistic manufacturing process characteristic, circuit

simulation is performed with temperature, voltage and process parameter over the range of values that are expected to occur. The critical values at process corner are simulated with minimum and maximum condition.

To exercise all input-to-output paths through the cells, input stimulus will be provided to the circuit simulator. Since many repetitive executions of the circuit simulator are required for each cell, the characterization is done using an automatic cell characterization tool.

6.0 Model development and documentation

After characterizing, the cells functional description and timing data are transformed to the format required by a specific design tools. Most design tools utilise special-purpose model formats with syntax for explicitly describing propagation delays, timing checks, and other aspects of cell behaviour that are required by the tool.

The final requirement is a documentation that summarises the functionality and timing of each cell. The functionality is frequently describe with truth table, and timing data is presented in a simple format in the datasheet. The documentation for each library contains:

a. setup and hold times
b. minimum cycle time, enable and disable time
c. truth table for small/medium complexity cells
d. operating range of temperature and voltage
e. fan-in and fan-out
f. variation of timing due to temperature and voltage
g. path delays
h. library cell symbol
i. timing diagrams.

7. Conclusion

As new technology arrives, IC design and manufacturing activities become more complex. In such environment, a successful design activity relies heavily on the ASIC library. The advantages of having library are faster time-to-market and reuse of often complex logic functions. This paper has presented a design flow for standard cell library done in MIMOS. The design methodology and requirement has been described. It is obvious that a very careful procedure and format has to be followed in order to produce a good cell library for ASIC design. Finally, modeling the silicon into the EDA tools play an important role to achieve accurate timing characteristic for the library, thus guarantee a working final product

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